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Development of Non-Volatile Semiconductor Memory

Final Report

March 16, 1979

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APPENDIX A.1

VOLATILE ORGANIC ANALYSIS

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REFERENCES

1. "Development of Non-Volatile Semiconductor Memory" Plan. Design and Development Program, March 5, 1976. Contract No. NAS 9-14881, DRL #T-1092A, Line Item 2, DRD #TM-241T.
2. "Development of Non-Volatile Semiconductor Memory" Report, Interim Progress, August 12, 1976. Contract No. NAS 9-14881, DRL #T-1092A, Line Item 2, DRD #TM-241T.
3. "Development of Non-Volatile Semiconductor Memory" package, Design Review Data, February 11, 1977. Contract No. NAS 9-14881, DRL #T-1092A, Line Item 3, DRD #CM-089T.
4. "Development of Non-Volatile Semiconductor Memory" Report, Interim Progress, February 11, 1977. Contract No. NAS 9-14881, DRL #T-1092A, Line Item 2, DRD #TM-241T.
5. Development of Non-Volatile Semiconductor Memory" Report, Interim Progress, September 23, 1977. Contract No. NAS 9-14881, DRL #T-1092A, Line Item 2, DRD #TM-241T.
6. "Development of Non-Volatile Semiconductor Memory" Report, Interim Progress, June 29, 1978. Contract No. NAS 9-14881, DRL #T-1092A, Line Item 2, DRD #TM-241T.
7. "Development of Non-Volatile Semiconductor Memory" Report, Interim Progress, December 11, 1978. Contract No. NAS 9-14881, DRL #T-1092A, Line Item 2, DRD #TM-241T.
8. "Non-Volatile Semiconductor Memory Development Study" Final Report, September 12, 1975. Contract No. NAS 9-14486, DRL #T-1092, Line Item 2, DRD #MA-183TB.

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Definitions

o	
A	Angstrom, 10^{-10} meter
A	Address, 8 per SU200
CMOS	Logic with 0 to +15 volt signal input or output
C/RW	Clear/Read Write control on SU200
DI	Data In, 8 per SU200
DIP	Dual In Line Package
DO	Data Out, 8 per SU200
DS	Data Strobe control on SU200
GND	Ground reference voltage on SU200
HYBRID	Module which contains 8 SU200 die
I/O	Input/Output
ME	Memory Enable Control on SU200
MNOS	Metal Nitride Oxide Silicon: non-volatile semiconductor technology
MOST	Metal Oxide Silicon Field Effect Transistor
mw	Milliwatt
pf	Picofarad
PS	Power Strobe control on SU200
RAM	Random Access Memory
ROW	MNOS transistors with a common gate line
R/W	Read Write control on SU200
S/D	Source and Drain nodes of a MOST
SiO ₂	Silicon Dioxide
SU200	2048 bit MNOS RAM
TE101	MNOS test chip
TUB	N-type silicon surrounded by p-diffusion ring
μs	Microsecond
V _{DD}	Negative voltage on SU200
V _R	Read reference voltage on SU200
V _{SS}	Positive voltage on SU200
V _T	MOST threshold voltage
Φ1	Clock control on SU200
Φ2	Internal clock on SU200
Φ2'	Internal clock on SU200

1.0 Abstract

This report documents the results of a 36-month Non-Volatile Semiconductor Memory Development program for a 2048 bit chip (SU200) and a 16,384 bit hybrid module. A 256 word by 8-bit Random Access Memory (RAM) chip was developed utilizing p channel, metal gate Metal-Nitride-Oxide-Silicon (MNOS) technology; with operational characteristics of a 2.5 microsecond read cycle, a 6.0 microsecond write cycle, 800 milliwatts of power dissipation; and retention characteristics of 10^8 read cycles before data refresh and 5000 hours of no power retention. The chip has an operational temperature range of -25°C to $+70^{\circ}\text{C}$, is packaged in a 40 pin Dual-In-Line-Package (DIP), requires +15, -4, -10 volts, has CMOS level control signals, and 2 PMOS level clock signals. A hybrid module was developed with an organization of 2048 words by 8 bits that is populated with six CMOS interface chips and eight SU200 die packaged in a 60 pin metal hybrid package with ceramic substrate. A microprocessor controlled memory exerciser was developed with support software to test both the DIP and Hybrid packages. The SU200 DIP package was subjected to MIL-STD-883 testing for purposes of evaluation.

The SU200 met the final statement of Work Requirement, however Read Access, Write Cycle, continuous Read Retention and operational temperature range were modified to reflect the realistic capabilities of P-channel MNOS in RAM applications. The original requirements of Capacity, Interfacing, Power Dissipation, and Input Protection were met. No radiation testing was performed.

Several design and process iterations were performed during the chip development phase of the program. A change in the process for the fixed gate transistor used in the control circuitry involved the utilization of a dual layer gate structure of nitride and oxide rather than oxide alone and provided for a less complex process and a more reliable gate with high break-down voltages. Design changes were implemented to reduce switching currents that caused parasitic bipolar transistors inherent in the MNOS structure to turn on. Final wafer runs exhibited acceptable yields for a die 250 mils on a side.

MIL-STD-883 evaluation testing was performed on the SU200 DIP packaged devices in order to determine the maturity of the device. Sixteen devices were subjected to the testing. The SU200 was found to have a fixed gate breakdown mechanism when operated continuously at high temperature. One of ten devices failed during test after temperature cycling, six of nine devices failed the 70°C burn-in and all 4 devices failed the 1000 hour operating life test.

The hybrid modules were tested and found to have no design or layout problems. Continuous operation of the hybrid modules did cause SU200 failures due to the fixed gate breakdown mechanism encountered in MIL-STD-883 testing. The gate breakdown was aggravated by heat build-up in the hybrid modules due to power dissipation by SU200 devices in the non-select state.

The SU200 does meet the revised statement of work requirements. However, future development work could address several tasks that would improve the producibility of the SU200. Specific development tasks would be to improve the fixed gate oxide growth process to make the oxide thicker and have improved breakdown integrity, to eliminate circuit power dissipation in an unselected state and other manufacturing technology related items to improve the yield.

2.0 Performance Specifications

2.1 Summary

The Statement of Work (SOW) requirements for the SU200 performance parameters are summarized in Table 2.1. The test data on the ten devices which met the final SOW requirements was delivered and substantiates the following performance parameters.

Specification	Initial Contract Requirements	Final Contract Requirements	Contract Goals
Capacity (bits)	2048	2048	2048
Access Time (us)	1.5	2.5	0.5
Write Time (us)	4.0	6.0	2.0
Retention (hrs.)	5000 continuous read	5000 storage (10^8 read cycles)	5000 continuous read
Operating Temperature (°C)	-55 to 125	-25 to 70	-55 to 125
Interfacing	CMOS Compatible	Signal I/O CMOS Compatible Vol- tages +15,0,-5, -10	CMOS Compatible
Power Dissipation (mw)	800	800	600
Radiation Resistance rads (Si)	----	Not Tested	10^6
Transient Protection	Forward and Re- verse breakdown voltage protec- tion on input signals	Forward and Re- verse breakdown voltage protec- tion on input signals	Forward and Re- verse breakdown voltage protec- tion on input signals

Table 2-1. Chip Performance Specification Summary

2.2 Capacity

The SU200 was designed with a 2048 bit capacity organized as 256 words by 8 bits. The memory array has two groups of 128 words each. Each memory bit is made up of 2 MNOS transistors, thereby giving the memory array a total of 4096 transistors.

2.3 Access Time

The SU200 meets the 2.5 microsecond (us) Access Time at -25°C to 70°C . The original SOW was 1.5 us at -55°C to 125°C .

2.4 Write Time

The SU200 meets the 6.0 us Write Time at -25°C to 70°C . The original SOW was 4.0 us at -55°C to 125°C .

2.5 Retention Time

The SU200 exhibits 10^8 read cycles before refresh with a 2.5 us read cycle and a 6.0 us write cycle over the temperature range of -25°C to $+70^{\circ}\text{C}$. The 5000 hour no power retention has been verified with a 2.5 us read cycle at 25°C .

2.6 Interfacing

The SU200 has CMOS compatible I/O signal levels. Power supply levels used on chips are +15, 0, -4, -10 volts. Two PMOS level clocks (+15 to -10 volts) provide chip selection and address initialization.

2.7 Power Dissipation

The SU200 meets the power dissipation requirement of 800 milliwatts (mw) or less over the temperature range of -25°C to $+70^{\circ}\text{C}$.

2.8 Input Protection

The SU200 has been designed with input protection circuitry on all signal inputs.

2.9 Operating Temperature

The SU200 meets the read access time, write time, power dissipation, and retention requirement simultaneously over the temperature range of -25°C to $+70^{\circ}\text{C}$. The original SOW was a 1.5 us read and a 4.0 us write at -55°C to 125°C .

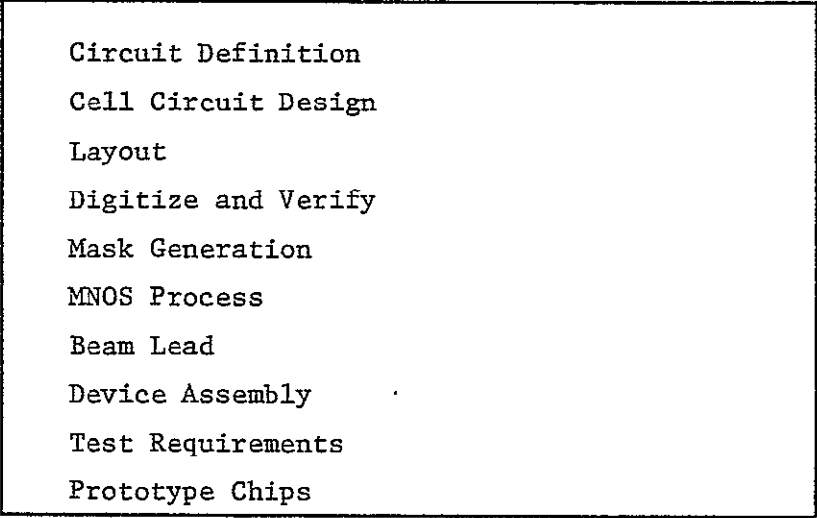
2.10 Radiation Resistance

The SU200 was designed utilizing a modified version of the Sperry Radiation Hard MNOS process. The full Sperry Radiation Hard MNOS process was initially tried on several lots but was eventually modified to eliminate removal of the fixed gate nitride. This was done since contract schedule; resources and SOW requirements didn't warrant excessive effort just to meet a contract goal. No radiation testing was done to determine the level of radiation resistance of the SU200.

3.0 Chip Development

3.1 Task Summary

The Chip Development task of the memory development program included the tasks shown in Figure 3.1.1.



- Circuit Definition
- Cell Circuit Design
- Layout
- Digitize and Verify
- Mask Generation
- MNOS Process
- Beam Lead
- Device Assembly
- Test Requirements
- Prototype Chips

Figure 3.1.1. Chip Development Tasks

The circuit definition, cell circuit design, layout, and digitize and verify tasks encompassed the chip design effort. The mask generation effort provided the interface between the design and processing. The MNOS process, beam lead, and device assembly were the chip fabrication tasks. Ten prototype chips were tested to and met final SOW requirements, however subsequent MIL-STD-883 test revealed a process related failure mechanism.

The 2048 bit MOS RAM (SU200) has a 256 word by 8-bit organization with each bit consisting of two memory transistors. As shown in the block diagram in Figure 3.1.2, the memory cells are partitioned into two isolated and independent memory tubs, each tub containing 128 8-bit words. Address selection is accomplished by decoding 128 row drivers while proper tub selection is made via the source drain control. As this implies, there are seven address pins required for decoding the rows. One additional address pin is required for decoding the source drain control which selects between the left and right pair of tubs. Separate data input and output pins were utilized. The total chip size is 250 by 250 square mils which is very close to the size indicated in the Statement of Work. A total of 34 pins is needed for operation of the RAM.

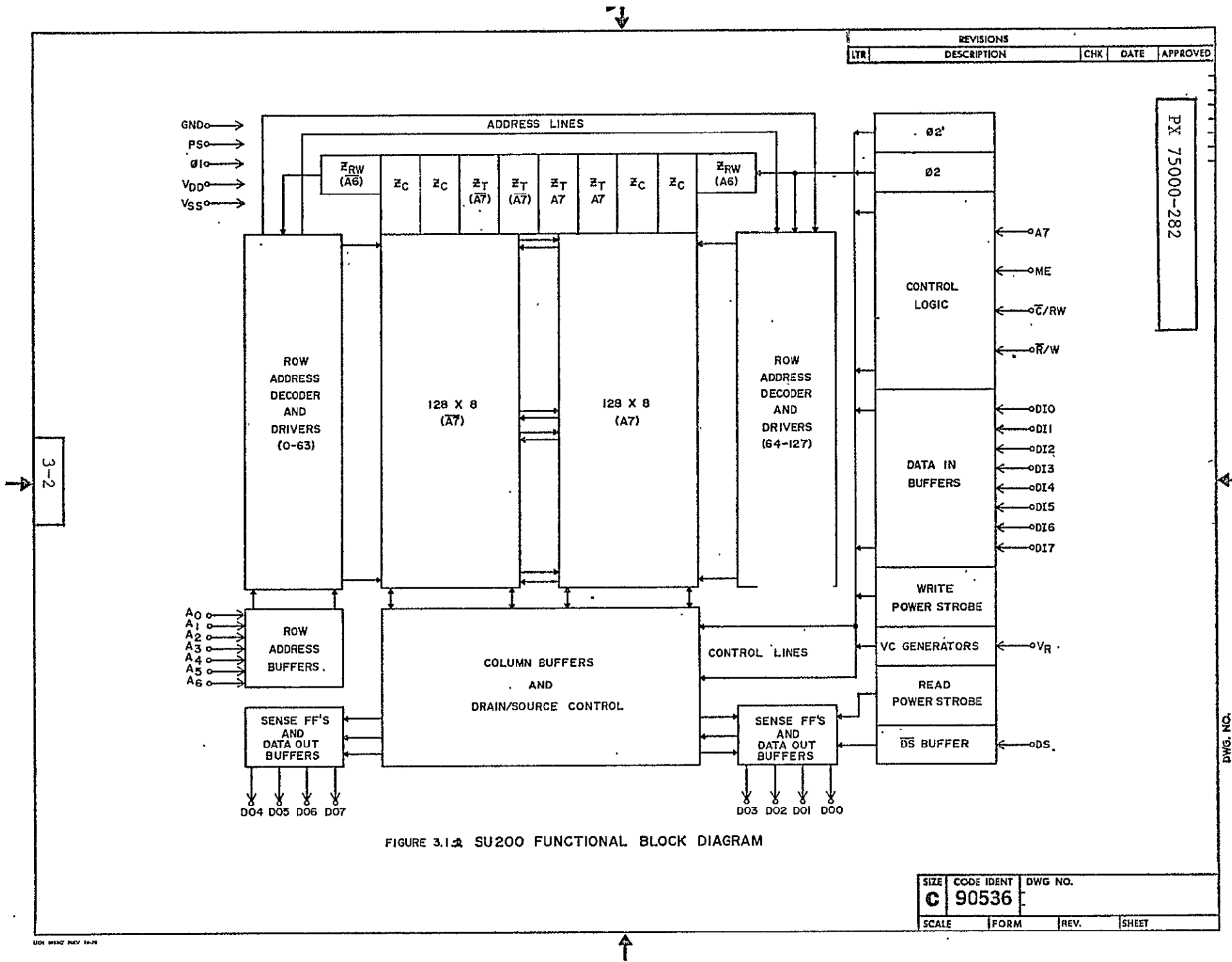


FIGURE 3.1-1 SU200 FUNCTIONAL BLOCK DIAGRAM

SIZE	CODE IDENT	DWG NO.
C	90536	
SCALE	FORM	REV.

3.2 Circuit Definition

Many of the circuits used in the SU200 were used repetitively and could be digitized just once and stepped into the overall layout. These circuits are listed in Table 3.2.

Table 3.2. SU200 Cell Count	
Circuit Type	Number Required
Sense Flip Flop and Data Out	8
Data In	8
Row Driver	128
Address Inverter (A_0 - A_6)	7
Source Drain Driver	32
Tub Driver	4
Clear Driver	4
ZRW Driver	2
VC Generator	2
Source Precharge	2
Source/Drain Control	2
Data Select	2
Memory Cell	2048

Following is a brief description of each circuit type used in the finalized design of the SU200. Circuit schematics are given in Appendix A.

Address Inverters (A_0 - A_6)

These circuits are bootstrapped inverters which drive push-pull outputs. They are used to drive the 1 of 128 nor row decoder. The output stage is tied to ground rather than V_{DD} to conserve power. The PS input is used to put the inverter at zero power during the standby mode.

Address Inverter (A_7)

This circuit is identical in function to the other address inverters. It is used to decode between the left and right side of the memory matrix.

Row Driver and Decoder

There are 128 row drivers, 64 on each side of the memory area. These circuits are used to selectively gate -10, 0, or +15 volts onto row lines. Initially, ϕ_1 pulses negative to -10 volts precharging the first two stages. During this same time frame, the address is set up. Now, if the address is selected, the first stage will remain at a negative voltage when ϕ_2 goes negative since there is no path to ground. This implies that the second stage will go to V_{SS} when ϕ_2' pulses. However, if the address is not selected, the first stage will go to V_{SS} upon the negative transition of ϕ_2 and the second stage will remain precharged. It should be noted that there must be enough delay between ϕ_2 and ϕ_2' to allow the first stage to swing to V_{SS} before ϕ_2' comes along. With everything now set up, reading or writing can take place. If Z_{RW} pulses on a selected row, the output will go to -10 volts in the case of a write and to 0 volts for a read. In both cases, for an unselected row it will remain at V_{SS} . The only power dissipated by this row driver is switching power meaning there will be zero standby power.

Source Precharge

This circuit, which also has a bootstrapped input stage driving a push pull output stage, is used to precharge the sources to 0 volts during a read. If \overline{R}/W is at +15 volts and \overline{C}/RW at 0 volts (signifying a read), the output of the circuit will go to $V_{DD} - V_T$. This drives the gate of a device which is part of the source/drain driver. This device transfers 0 volts to the sources of all the memory transistors. Now, in the case of the selected side of the memory, the address signal ($A7/\overline{A7}$) will be on and when $ZRW1$ or $ZRW2$ goes negative, the source precharge output will go to V_{SS} . If not selected, the source precharge signal will remain negative until \overline{C}/RW changes states. It is important in the case of a selected side for the signal to go to V_{SS} so the VC generator can take control of the source.

Drain Precharge

This circuit performs the same function as an unselected source precharge circuit. During a read, the drains of all the memory transistor are driven to 0 volts and held there throughout the duration of the cycle. This circuit is at V_{SS} during the complete write cycle.

Source/Drain Control

This circuit is responsible for allowing data to be steered into the drain and sources of a memory transistor during a write. During a read cycle, the drain precharge signal will be on implying that the S/D control output will be a V_{SS} . During a write, the source/drain control will go to 0 volts for the selected side and will remain at +15V for the unselected side. The write power strobe signal is used to enable address control during a write cycle.

Source-Drain Driver

The source-drain driver consists of all the control gates for correct operation of the drains and sources during any mode of operation. The drain precharge, source precharge, data select and VC gates turn on only during the read cycle and are out of the picture during a write. The S/D control and data in gates allow data to be steered in when writing. As the source-drain bootstraps are used only during the write cycle, they are controlled by write power strobe. During the clear portion of the cycle, all the drains and sources will go to -10 volts. Depending on whether data is high or low, these modes will be pulled to V_{SS} or remain at V_{DD} during the write portion of the cycle.

Data Select

This circuit's function is to allow data from the selected side of the memory matrix to be transferred to the sense amps. It turns on only during the read cycle.

Data In Buffer

The data in buffer is responsible for buffering data and its complement and providing them as inputs to the source-drain driver. The write power strobe input is used for power saving during the read cycle and also during the initial portion of the write cycle. Both the DATA and $\overline{\text{DATA}}$ outputs are at +15 volts during the clear portion of the write cycle due to the $\overline{\text{C/RW}}$ signal being at 0 volts. Sometime during this portion of the cycle data it must become valid. Immediate \bar{y} upon the return of $\overline{\text{C/RW}}$ to +15 volts, signifying the beginning of the write portion of the cycle, DATA and $\overline{\text{DATA}}$ will go to their correct states.

VC Generator

The VC generator provides a technique for maximizing the retention of the MNOS memory element by minimizing the read disturb (difference between V_{GS} and V_{TT}). The bottom push-pull circuit selects which VC generator should become active. To become active, the inhibit device must have its gate go to +15 volts. The first stage of the upper circuit provides an output voltage which is independent of variation in threshold voltage. This voltage feeds the second section which provides a constant turn-on voltage to the VC transistor in the S/D driver. During the read cycle, R.P.S goes negative powering up the VC generator and allowing selection. If the inhibit device is off, the device in the source-drain driver turns on slightly and there is a resistive path to V_{SS} through it from the memory transistor. This pair of transistors (memory transistor and VC transistor of S/D driver) can be thought of as a voltage divider. Depending on what the variable threshold of the memory transistor is, the ratio of the resistances of the two devices changes. If the threshold of the memory transistor is more negative, it becomes a high impedance device and the saturated output will be closer to V_{SS} than if the variable threshold was more positive. As one transistor in each bit pair is in the cleared state and the other in the written state,

the difference in these thresholds can be detected in the manner just described by using a sense flip-flop.

Sense Amp and Output Buffer

The sense amp receives two input signals from the output of the voltage divider circuits described in the VC generator section, interrogates these signals and provides the appropriate voltages to the output buffer. Both the sense amp and output buffer are powered up by the read power strobe. During the write cycle, they are in a zero power state. The \overline{DS} signal pre-charges all output nodes to +15 volts initially during the read cycle. The signals from the memory (DATA and \overline{DATA}) are fed in now and upon the positive transition of \overline{DS} , the flip-flop will sense the difference in V_{TTS} and switch to the appropriate state. The output buffer does exactly what its name implies: it buffers the signals from the sense amp to the DATA OUT pin. The output is CMOS compatible and was designed to drive a 50 pf load in 50 nsec.

Data Strobe Buffer

The data strobe buffer is a bootstrapped inverter driving a push-pull output. Its function is to precharge the sense flip-flops and output buffers to +15 volts during the read cycle. When data strobe changes state, the sense flip-flop can switch to the correct state.

Power Strobe Buffer

This buffer is used to produce the complement of power strobe. The signal's function is in discharging the bootstrapped nodes of all the high capacitance drivers when the chip is in the standby mode.

Read/Write Buffer

The read/write buffer is used for generating the complement of the $\overline{R/W}$ signal. The output of this circuit will be at 0 volts during the read cycle at +15 volts during a write. The power strobe input is used to eliminate any standby power.

Clear/Read Write Buffer

This circuit is a push-pull inverter which generates the complement of the $\overline{C/RW}$ signal. Its output will be at V_{GS} during read and write operations and at 0 volts during a clear operation. The power strobe input is again used to eliminate standby power.

Control for Read Power Strobe

The read power strobe output will go to +15 volts during the read cycle and will otherwise be at 0 volts. The $\overline{R/W}$ signal will go to 0 volts immediately upon the beginning of the read cycle and the output of the R.PS control will actually go to 0 volts when 02 comes on. Since the signal isn't needed

immediately at the start of the cycle, the $\Phi 2$ input is used for power reduction since R.PS control is not needed until this time.

Tub Driver Control

This circuit essentially serves the same purpose as the read power strobe control except that it is used for the tub drivers. The first stage selects which two of the four tub drivers will be enabled. With this information set up at the gates of the push-pull stage, the tub driver control output can switch to the appropriate state when the ME signal goes to 0 volts.

Clear Driver Control

The clear driver control operates in exactly the same manner as the tub driver control. When ME goes to 0 volts during the write cycle, the 4 ZC drivers will be selected.

Control for the ZRW Driver

Again, this circuit is very similar to the tub driver control. One of two ZRW drivers is selected during the read and write operations. The initial stage is set up before ME goes to 0 volts and when ME does make its transition the output becomes valid.

$\Phi 2$ and $\Phi 2^1$ Drivers

These are very important signals in setting up the row addresses. As both $\Phi 2$ and $\Phi 2^1$ must drive larger than normal MOS loads, two stages of bootstrapping are used. The second stage has much more drive capability than the first and is able to drive a large load to V_{DD} in a short time. The source follower circuit which feeds the $\Phi 2^1$ driver is a delay circuit which introduces enough of a time delay for the first stage of the row driver to set up before $\Phi 2^1$ becomes active. Both of these signals are generated off the rising edge of $\Phi 1$.

Read Power Strobe

The read power strobe is used to power up many of the key circuits used during the read cycle. Its main purpose is to reduce power during the write cycle by powering down circuits which are utilized only for the specific purpose of reading. The control circuitry on the initial bootstrap node is for discharging this node when it is not selected. It should be noted that this node is precharged originally by $\Phi 1$. One of the transistors on the output stage has its substrate tied to its source. This circuit technique eliminates body effect, thereby enhancing performance by reducing response time.

Write Power Strobe

The write power strobe serves the same function during the write cycle as the read power strobe served during the read cycle. Circuits used only during the write operation are powered down resulting in a large reduction in power dissipation during the read cycle.

Tub Driver

The tub driver utilizes three stages of bootstrapping because of the large load it must drive. During a clear operation, this buffer is responsible for driving the selected tub to -15 volts in as short a time as possible. Again, the output transistor has its source and substrate tied together in order to optimize the circuit's performance.

ZC Driver

The ZC driver operates in the same manner as the tub driver. It is responsible for driving 31-row lines to -15 volts during a clear operation. This circuit must make its negative transition at the same time as the tub driver. As it drives more capacitance than the tub driver, its device sizes are scaled up accordingly.

Read Section of ZRW Driver

The ZR driver is responsible for driving the selected row line to 0 volts during a read operation. It utilizes two stages of bootstrapping and is not active during the write cycle.

Write Section of ZRW Driver

This circuit is nearly identical to the ZC driver. Its purpose is to drive the selected row line to -10 volts during a write operation. The ZW driver is inactive during the read and clear operations.

3.3 Cell Circuit Design

3.3.1 Interfacing

Figure 3.3.1 shows a pin out of the SU200. As shown, four voltages are required: +15, -10, 0, -4. Two 25-volt signals with rise and fall times of 50 nsec are required: $\Phi 1$ and PS. The input capacitances for these signals are 15 pfs and 50 pfs, respectively. Four 15-volt control signals with rise and fall times of 50 nsec are required: DS, $\overline{R/W}$, $\overline{C/RW}$, and ME. Also as inputs, 8 address pins (A0-A7) and 8 data in pins (DI₀ - DI₇) are required. All of the control, address and data in pins have input capacitances of 5 pfs. The 8 data out pins (DO₀ - DO₇) are capable of driving 50 pfs in 50 nsec.

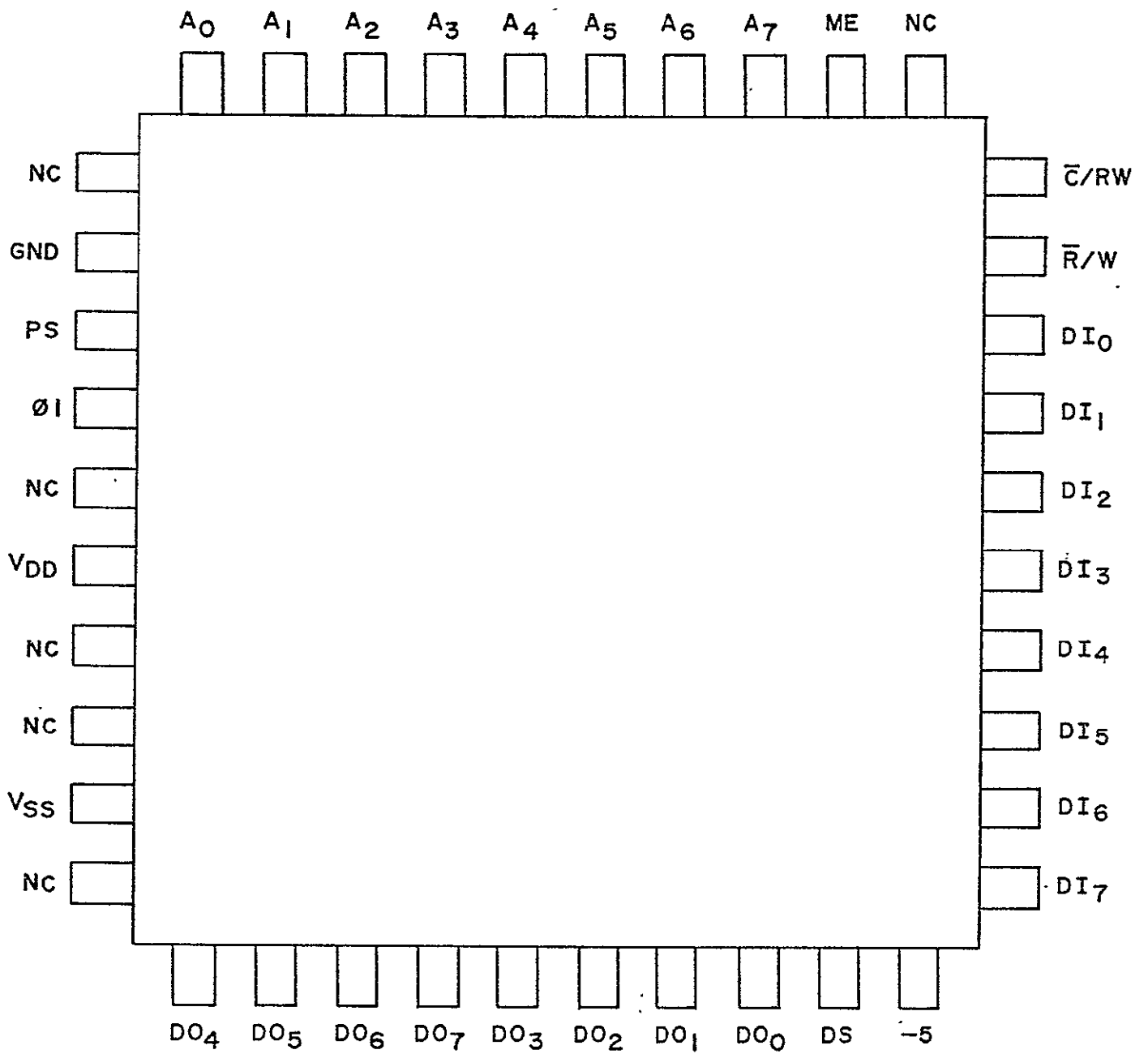


FIGURE 3.3.1: CHIP I/O PINS

3.3.2 Computer-Aided Design

Device functionality over temperature range was assured by the design of circuits which are tolerant to variations in threshold voltage, gain, Fermi potential, and intrinsic concentration. Computer-aided circuit analysis using temperature dependent model parameters as indicated in Table 3.3.1 was used for verification.

Table 3.3.1. Temperature Dependent Terms

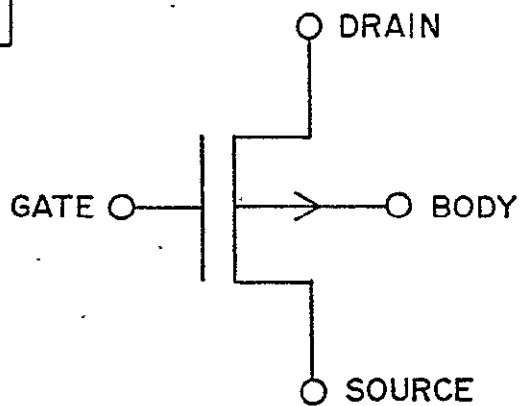
<u>Parameter</u>	<u>Symbol</u>	<u>Temperature Function</u>
Fixed Threshold Voltage	VTH	$V_{TH}(T) = V_{TH} + TV_{TH} (T-298)$ where TV_{TH} = empirical coefficient
Current Gain	BO	$BO(T) = BO (T-298)^{-3/2}$ where BO = gain at 298° K
Intrinsic Concentration	NI	$NI(T) = 6.8 \times 10^{15} T^{3/2} e^{(6430/T)}$
Fermi Potential	Φ_F	$\Phi_F(T) = \frac{KT}{q} \ln (N/NI(T))$

Since increasing temperature implies higher threshold voltage and lower gain, the +125°C limit was used as a worst-case for speed requirements and the -55°C limit, which implies low threshold and high gain, was used as the worst case for power requirements.

The computer-aided analysis program used to verify circuit operation was Sperry Univac's version of the Transient Analysis Program. This program uses component models based on processing parameters which have been determined to be specifically relevant to the Sperry MNOS radiation hard process. Table 3.3.2 lists the important processing parameters which must be used in the Transient Analysis Program to simulate correct circuit operation. Figure 3.3.2 shows the actual circuit model employed for an MOS device by the program, and Figure 3.3.3 shows where the parasitic capacitances are physically located on a device.

Definition		Nominal Value	Units
t_{ox}	Gate Oxide Thickness	1000	A
V_{TH}	Threshold Voltage: Fixed Variable	2 to 3 1 to 15	volts
RP	P-Diffusion Resistivity	50	ohms/square
CG	Gate Capacitance: Fixed Variable	46.5×10^3 172×10^3	pF/cm ²
BO	Current Gain: Fixed Variable	7 18	umhos/volt
CJO	Junction Capacitance	15.5×10^3	pF/cm ²
COV	Overlap Capacitance	18.1	pF/cm
ϕ	Mobility Reduction Factor	.02	volt ⁻¹
CE	Back Bias Constant	.5	
NEXP	Depletion Capacitance Exponent	.5	
S	Surface Mobility	180 to 200	cm ² /volt-sec
V_{TF}	Parasitic Threshold Voltage	40	volts
TVTH	Threshold Variation Due to Temp.	2.4	mV/oK

Table 3.3.2. Process Parameters Used in Computer Analysis



CIRCUIT SYMBOL FOR A P CHANNEL ENHANCEMENT MODE MOST

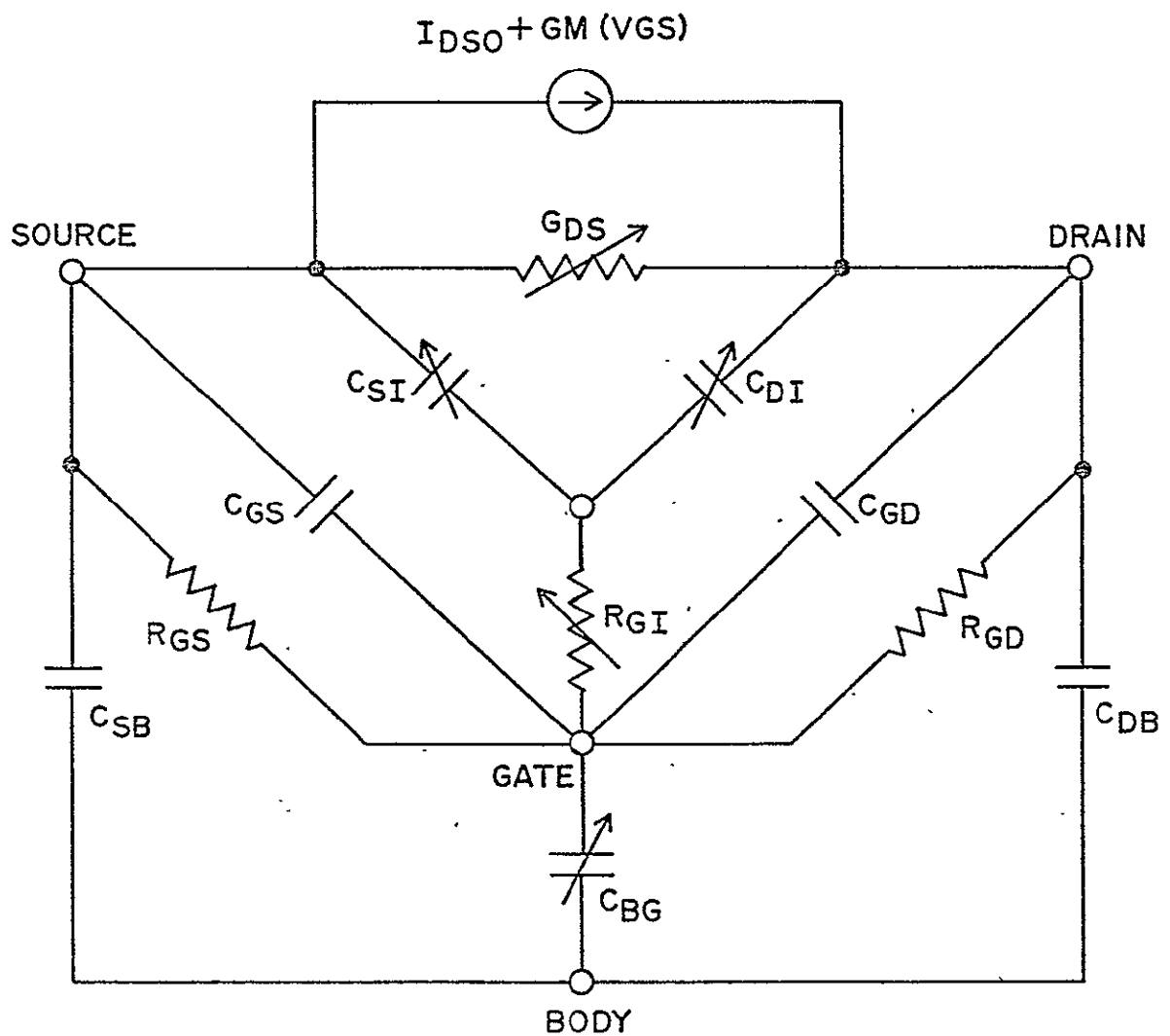


FIGURE 3.3.2: P CHANNEL MOST MODEL SCHEMATIC

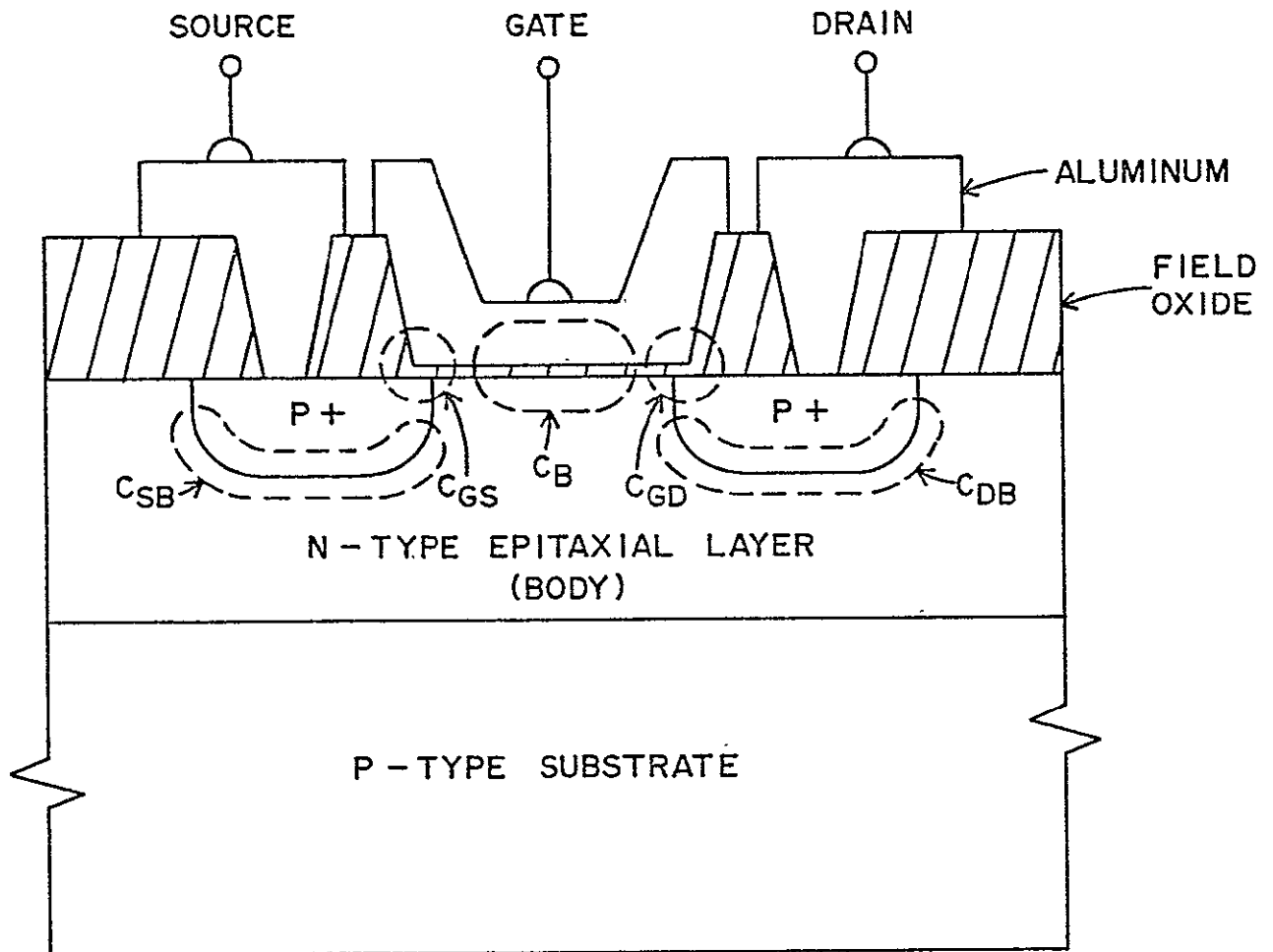


FIGURE 3.3.3: PHYSICAL CONSTRUCTION OF A P CHANNEL MOST

3.3.3 Memory Gate Selection

The radiation hard MNOS memory transistor was chosen over the step gate transistor in the design of the 2048 bit MNOS RAM. In addition to allowing the final product to be radiation hard, the chosen gate structure has many other advantages with respect to reducing chip size. These include:

- 1) Reduced cell size - The minimum dimensions for the radiation hard gate is $8\mu \times 10\mu$. This is compared to a minimum of $14\mu \times 14\mu$ for the step gate cell.
2. Reduced capacitance - The capacitance per gate for the radiation hard cell is .148 pfs as compared to .165 pfs for the step gate structure. This may seem insignificant, but when you take into account that each row driver drives 32 gates, it becomes very significant.
- 3) Increased current gain - The step gate structure is effectively two fixed transistors in series with a variable transistor. An effective gain of 10 results. The radiation hard gate has a gain of 18.

What all this means is an overall reduction in chip size. A larger current gain factor along with a smaller minimum length means that significantly less area is required in the actual memory array. This implies a smaller tub which means the tub drivers will not be required to drive as large a load allowing them to be made smaller. Also, the reduction in gate capacitance makes a reduction in each of the 128-row driver sizes possible, thereby reducing peripheral circuitry area.

A topographical view of the radiation hard gate is shown in Figure 5-1. The radiation hard memory gate does not use the step gate structure which gives an added layer of oxide between the gate and the source/drain diffusion edges in the channel. The step gate structure eliminated the breakdown problem between the gate and source/drain diffusions which existed in the early development of MNOS structures. The breakdown mechanism was caused by nitride thinning at the bottom edge of the field oxide gate cut. The radiation hard gate uses a glass layer to increase the effective thickness at the edges of the gate region. The glass does not extend over the memory gate channel and thus does not affect the memory gain, capacity or radiation hardness, but does alleviate the breakdown problem.

The retention of the radiation hard gate cannot be directly predicted, but must be determined by actual circuit analysis. However, the 5000-hour no power retention requirement has been attained. The SU200 has a radiation hard memory gate structure but not a radiation hard fixed gate. Specific circuit implementations are the use of a two transistor memory cell which allows differential sensing of threshold differences of 0.1 volt between the two memory transistors. The implementation of a constant current sensing technique minimizes the read disturb on the memory transistor threshold.

MEMORY GATE STRUCTURE

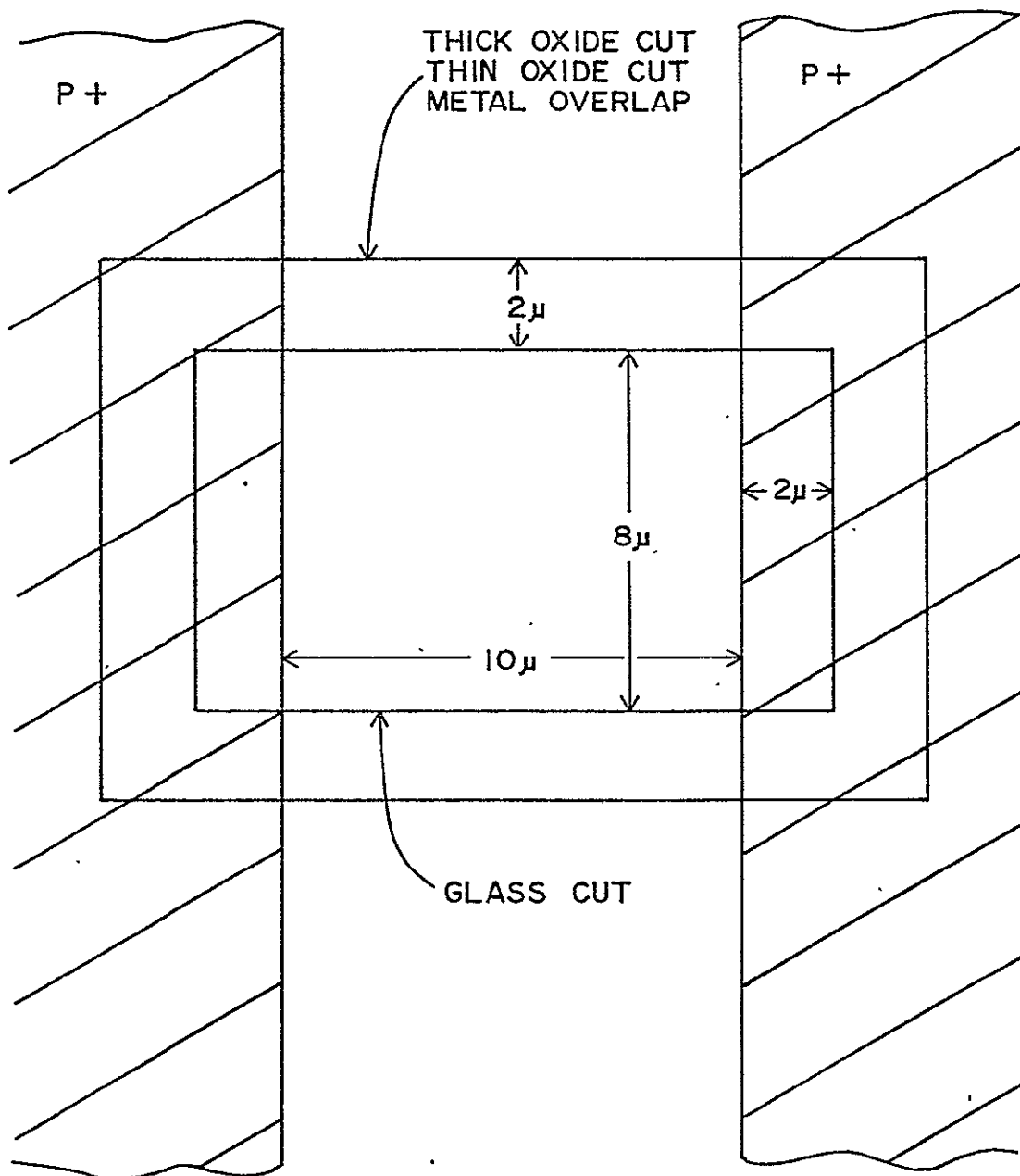


FIGURE 3.3.4: TOP VIEW RADIATION HARD GATE

3.3.4 Read Operation

The read operation is initiated when PS and $\phi 1$ go negative. PS selects the chip and allows the correct address to be selected. The $\phi 1$ signal is responsible for precharging the row drivers and also for internally generating $\phi 2$ and $\phi 2^1$. These two signals allow the completion of row driver setup. If the \bar{R}/W line is at V_{SS} , which signifies a read operation, the memory transistor drains and sources are precharged to 0 volts. The ME signal now becomes active, causing the selected ZR line to go to 0 volts. This, in effect, causes a complete row of memory transistors to have their gates charged to 0 volts. It is important that the drains and sources are precharged prior to the gate or there would be a disturb condition. It should also be noted that when \bar{R}/W is at V_{SS} and $\phi 2$ goes negative, read power strobe becomes active and goes to -10 volts. This signal enables the VC generators, sense flip-flops, and data out buffers. The drains of all memory transistors remain at 0 volts through the duration of the read cycle as do the sources of the transistors in the unselected tub. However, in the case of the selected tub, the source/drain control goes positive and the appropriate VC generator becomes active taking over control of the selected sources. This causes the sources to begin ramping toward +15 volts. As there are two memory transistors per bit, one will have a more negative threshold than the other. The voltage at the source of the transistor with the more negative threshold will saturate at a more positive source voltage than its counterpart. This difference in the voltages at the two sources is sufficient to enable the sense flip-flop to make a decision and switch to the appropriate state. The sense flip-flops will make their decision when DS goes positive and the data out drivers will buffer this information to the output pins.

The design was done to insure that under worst case conditions, the access time would be less than 1.5 microseconds. Included in the criteria for worst case conditions is high temperature, worst case processing parameters, and a small V_{TT} window.

3.3.5 Write Operation

During the write cycle, two independent actions take place. The first half of the cycle is utilized in clearing all 8 bits of the selected word while the second half of the cycle is used to write the appropriate data into the selected V_{TT} transistors. This entails leaving one transistor in each pair in the cleared state while the other transistor is written to a more negative threshold.

The row addresses are set up during the write cycle in the same manner as previously described in the read operation description. In this mode of operation the \bar{R}/W line goes to 0 volts, enabling the write power strobe which in turn precharges the source-drain bootstraps. During the clear

portion of the write cycle, \overline{C}/RW remains at +15 volts. This condition, coupled with the ME signal going to 0 volts, allows the selected ZC and ZT drivers to swing to -10V. This is a necessary condition since the n-type substrate cannot go more negative than the p-type drains and sources or there will be forward biased p-n junctions causing injection. The selected row line will remain at +15V while the other 127-row lines driven by the selected ZC drivers will go to -10V.

The logic is set up such that if a row is selected, the corresponding ZC driver is automatically selected. Also, the logic insures that a tub driver cannot be selected if the appropriate row is not selected. This leaves four possible combinations of voltages on the gate, drain, source and substrate of a memory transistor during a clear. These are described below:

- 1) Row selected, tub selected - The gate of the device will be at +15 volts and the drain, source, and substrate will be at -10 volts. This will cause the V_{TT} transistor to be put into the cleared or more positive threshold state.
- 2) Row selected, tub nonselected - The gate and substrate will be at +15 volts and the drain and source will be at -10 volts. The state of the memory transistor will not change.
- 3) Row nonselected, tub selected - The gate, drain, source and substrate will be at -10 volts. The state of the memory transistor will not change under these conditions.
- 4) Row nonselected, tub nonselected - The substrate will be at +15 volts and the gate, drain and source will be at -10 volts. This will introduce a channel shield effect and the state of the device will remain the same.

Even though data will not reach the sources and drains during the clear portion of the write cycle, the data in pins must become valid sometime during this period. ME will return to +15 volts causing the active ZT and ZC drivers to return to +15 volts. The ZC drivers going to +15 volts implies that all the row lines will also return to +15 volts. Now, the \overline{C}/RW line goes to 0 volts signifying the start of the write portion of the cycle. This signal also allows data to be transferred to the data in control transistor of the source-drain driver. ME will go to 0 volts switching the selected ZW driver to its active state. The selected row line will follow the ZW driver in its negative transition to -10 volts. The source drain control will go to V_{SS} in the unselected portion of the chip meaning that these sources and drains will remain at -10 volts. The selected portion of the chip's source drain control lines will go to 0 volts allowing the correct data to be steered through. In this case, the drains and sources will either remain at -10 volts if a more positive V_{TT} is desired or will go to +15 volts if a more negative V_{TT} is desired.

The substrate is always +15 volts during a write. The logic has been designed so there are four possible conditions on the nodes of the memory transistor during a write pulse. Following is a description of these possibilities:

- 1) Selected row, selected source-drain driver - The gate of the device will be at -10 volts while the source and drain will be at +15 volts. This condition will cause the transistor to be written into the negative V_{TT} state.
- 2) Selected row, nonselected source drain driver - The gate, drain and source of the device will be at -10 volts. This will introduce a channel shield effect and the memory transistor will remain in its present state.
- 3) Nonselected row, selected source drain driver - The gate, drain and source will be at +15 volts. The state of the memory device will not change.
- 4) Nonselected row, nonselected source drain driver - The gate will be at +15 volts and the drain and source will be at -10 volts. Again, the state of the memory transistor will remain unchanged.

3.4 Layout

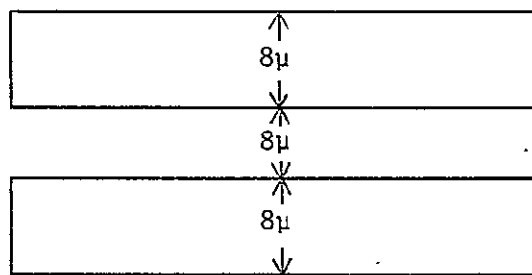
The SU200 layout was accomplished by hand layout of individual cells while following a chip layout plan for cell placement and voltage routing. The Sperry Radiation hard process design rules were followed. Extra mask levels were incorporated to allow for some process modifications which eventually were implemented in the SU200 process. Key design rules are shown in Figure 3.4.

3.5 Digitize and Verify

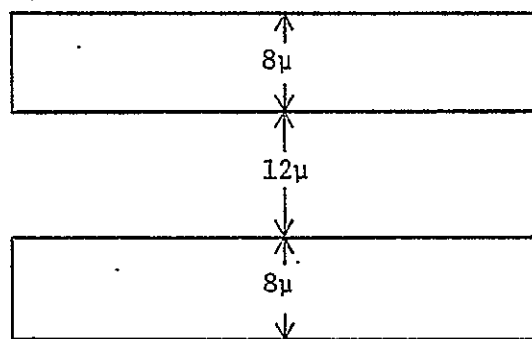
This task was accomplished through the use of the Applicon Interactive Graphics System.

3.6 Mask Generation

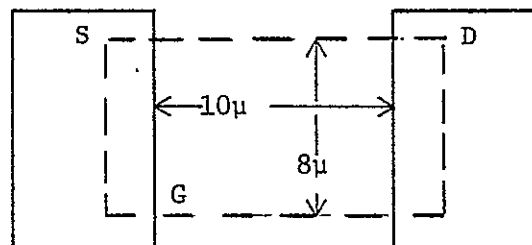
The masks were made in the Sperry Univac mask making facility. The availability of this facility allowed for rapid turnaround of initial design and design changes. The quality of masks was comparable to or better than industry standards.



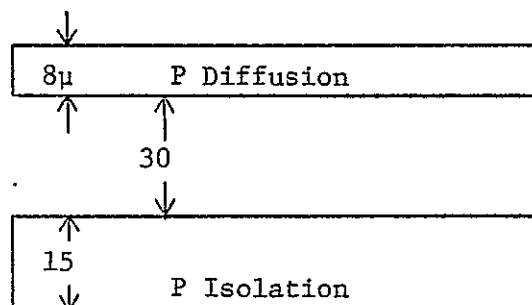
Minimum Metal Width and Spacing



Minimum P Diffusion Width and Spacing



Minimum Fixed Gate Length and Width



Minimum P Isolation Width and Spacing to P Diffusion

Figure 3.4. Key Design Rules

3.7 MNOS Process

3.7.1 Process Description

Starting Material

P-type substrate with 15 micron thick, three ohm-centimeter, 100 crystal, n-type epitaxial layer.

1. P isolation diffusion through epitaxy to contact p-substrate.
2. N⁺ diffusion for contact to n-tubs.
3. Source, drain, and interconnect with p⁺ diffusion.
4. Combination etch through field insulator to define fixed gates, variable gates and contacts.
5. Removal of about 500 Å grown oxide from variable gate and contacts.
6. Removal of about 500 Å variable nitride from contact areas.
7. Aluminum gate, contact and interconnect definition.
8. Removal of glass passivation layer from bond pads.

Process Steps

The baseline for the MNOS process consists of thirty-two steps, including three diffusions and eight photoresist masking operations. This process is to be the baseline process for the SU200 memory array.

The baseline process is shown in the process flow chart in Figure 3.7.1. A cross section of the final circuit is shown in Figure 3.7.2.

3.7.2 Wafer Run Analysis

The Sperry radiation hard MNOS wafer process was initially selected for the SU200 2048 bit MNOS RAM. Processing masks were obtained in February 1977 and processing was initiated. Several process runs were completed and analyzed. Results from the wafer analysis are discussed along with the process modifications.

Wafer Run EC3

EC3 was the first fully processed SU200 wafer run. All of the memory array subcircuits were analyzed for correct logic function and proper voltage levels. All of the subcircuits operated in the proper logical sequence except the tub drivers which were found to have a metal mask error shorting the output to the V_{DD} supply line. A mask change, 7_b, was implemented to correct the error. The wafers exhibited low fixed gate source/drain breakdown and high fixed gate thresholds. The gate and contact cuts through the field oxynitride were found to give much larger openings than defined by the mask. Experiments were started to minimize the field cut overetch and to determine the cause of the high thresholds.

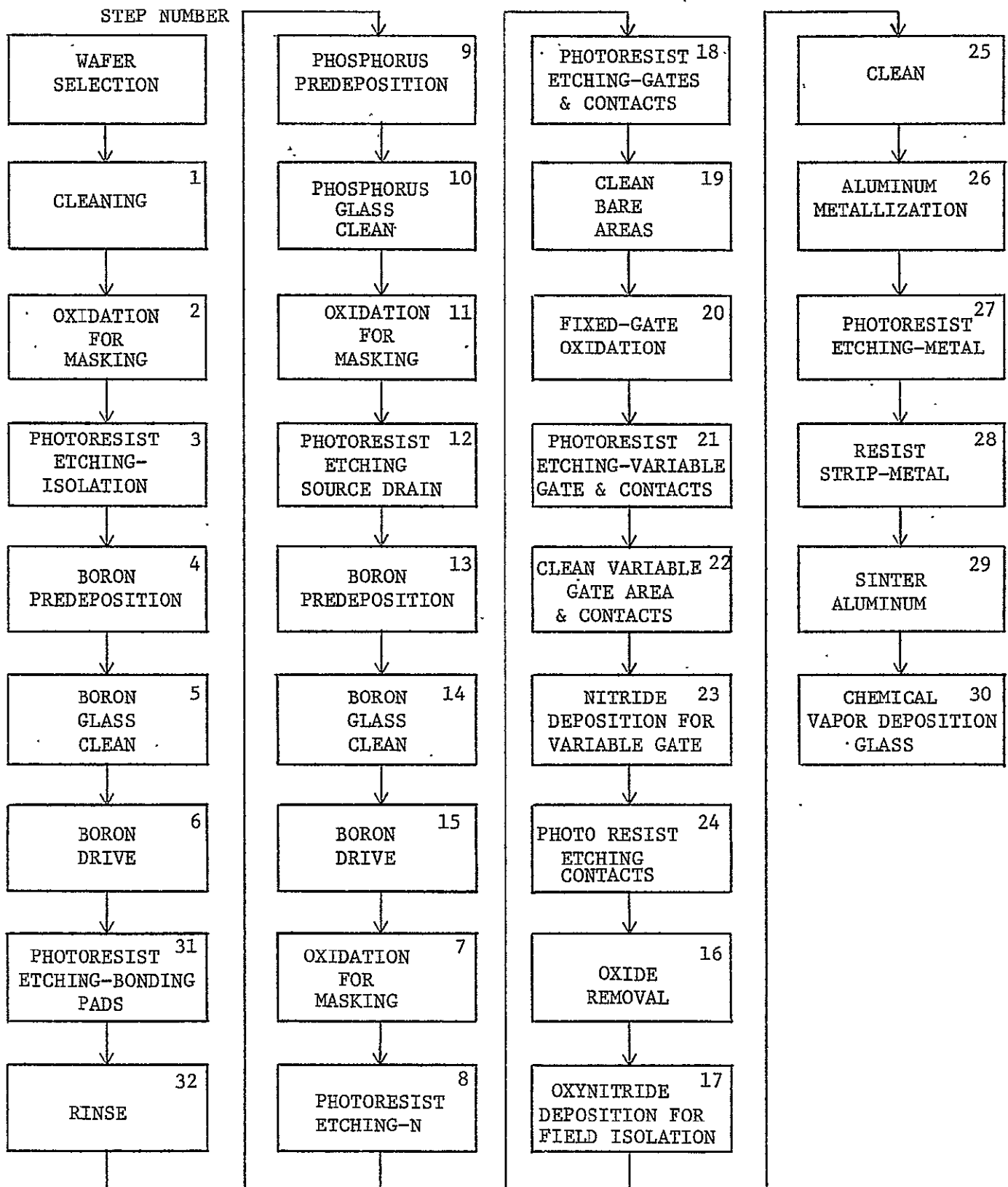
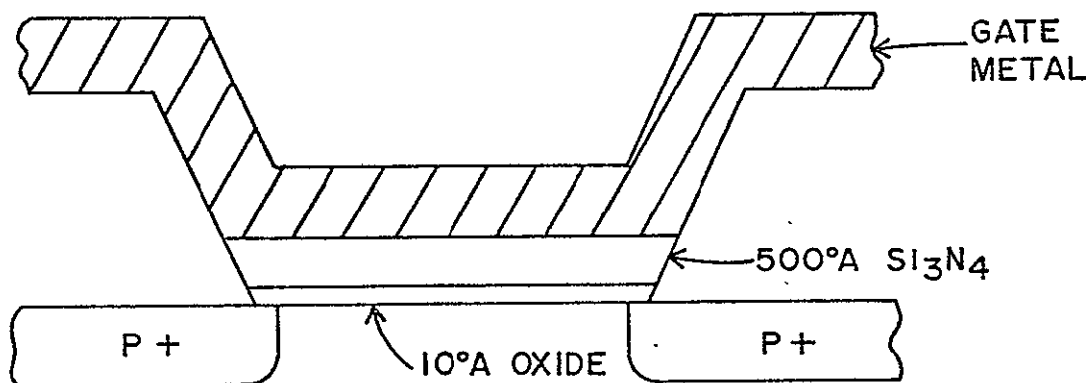
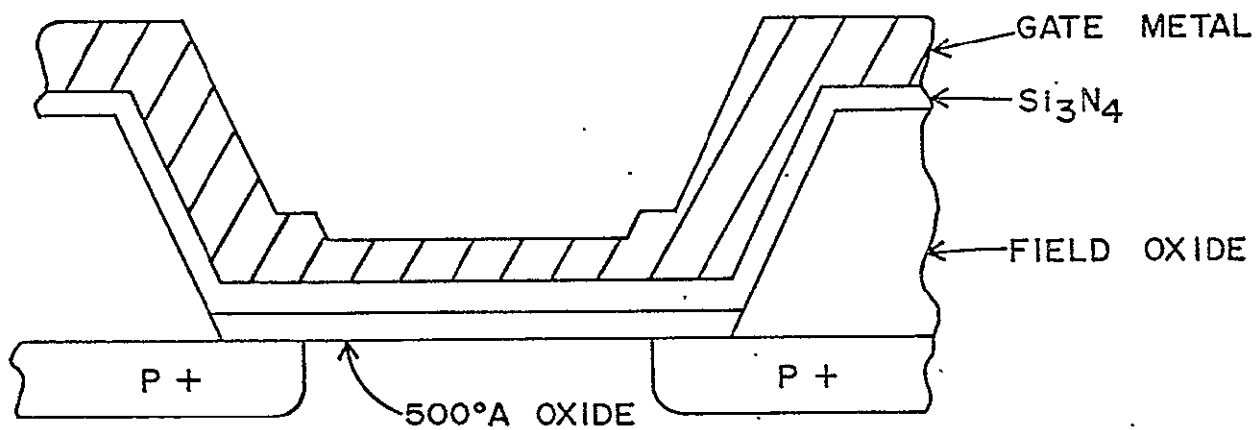


Figure 3.7.1. Process Flow Sperry MNOS Baseline Process



VARIABLE TRANSISTOR



FIXED TRANSISTOR

FIGURE 3.7.2 SU200 GATE STRUCTURE

Wafer Run EB1

EB1 came through processing immediately after EC3 and exhibited the same characteristics.

Wafer Run EC4

EC4 used the revised metal mask 7_b, which allowed the tub drivers to perform properly, thus verifying the functionality of the SU200 design. Run EC4 was split into 2 lots. One lot received the radiation hard process with the nitride removed from the fixed gates but with a thinner gate oxide in order to lower the threshold. This lot had lower thresholds, but the low fixed gate breakdown mechanism was still evident. The second lot was processed without removing the nitride from the fixed gates and with the thinner fixed gate oxide. This lot exhibited lower thresholds and higher breakdown voltages. Based on information obtained on this run, two probable causes for the fixed gate breakdown were postulated. The first cause was the process step which removes the nitride from the fixed gate. The gate may have been overetched or the etchant affected the fixed gate in some manner. The second cause was found to be deeper source/drain junction depths than expected in the design. The fixed gate thresholds were lowered due to the thinner gate oxides; however, the previous high thresholds were due to higher than expected Q_{SS} levels in the gate.

The previous problem of overetch of the field cut could not be compensated for in the process; therefore, processing masks 4, 5, and 6 were changed to shrink the field cut openings. Another mask set, level 11, was generated to facilitate experiments in which the non-radiation hard fixed gate would be used. Mask 1 was also changed in order to electrically isolate alignment marks and revision letters.

The deep source/drain junctions were caused by the high temperatures used during the fixed gate thermal oxidation. The solution to the problem was to not drive the junctions as deep during the source/drain reoxidation. The combined effect of the source/drain reoxidation and the thermal oxide fixed gate oxidation would give the proper junction depth.

An exact determination of the cause of the problem in the fixed gates due to the nitride etch could not be made; however, experimentation with the etchant concentrations and etch rates were performed.

The problem of the high fixed gate thresholds due to high Q_{SS} levels was felt could be solved by improved cleaning techniques, which would then lower Q_{SS} .

Wafer Run C12

C12 received the radiation hard process with the etching of the nitride from the fixed gates. The run exhibited the high threshold along with the low fixed gate source/drain breakdown. This run did have all of the mask changes implemented. C12 also had a low gate to source/drain rupture on the fixed and variable gates which was destructive.

The problems due to the nitride etch were still in evidence. It was then decided to process all new runs with a thinner fixed gate oxide and leave the nitride on the fixed gates. This would allow functional devices to be obtained sooner and thus give an opportunity to fully characterize the SU200.

The problem of the gate to source/drain rupture on the fixed and variable gates was attributed to the technique used for the cut through the field oxynitride. The etching mask was changed from metal to polysilicon and a chemical etch was used instead of a plasma etch.

Wafer Run C13

C13 received essentially the same process steps as C12 and had the same results.

Wafer Run C18

C18 received the non-radiation hard process and had threshold and breakdown voltages within design specifications. The problem of low gate rupture voltages was eliminated. The C18 wafer had partial memory action on 10 of 80 die analyzed. Also the high voltage drivers on the chip had full V_{SS} to V_{DD} signal swings which indicated the high fixed gate source/drain breakdown. The following runs were processed in a similar manner with emphasis placed on fine tuning each process step.

Wafer Run C21, C24

A design error was found that created a parasitic npn transistor between memory tubs which had common source/drain lines. The effect of the transistor was to short the tubs together during a clear causing the unselected tub to closely follow the selected tub during switching. A metal mask change 7c was implemented. The SU200 characteristics were much improved over previous runs. The high voltage on chip drivers had full voltage swings which is indicative of high breakdown voltages.

Wafer Runs C23, C25

These two wafer runs were processed with mask 7c. 36 dice with ammonia-silane ratio of 1500:1 and 18 dice with ammonia-silane ratio of 200:1 were found to be fully functional. The 7c mask change causes the memory to have two tubs of 128 words by 8 bits each.

Wafer Runs C26, C27

Evaluation of the two runs identified a problem of a voltage gradient across the n-epi layer under the control circuitry caused by S/D leakage currents. The voltage drop in the epi layer is large enough to cause parasitic P-N-P transistors to turn on. The parasitic transistors, in turn, discharge precharged capacitors in the write circuitry of the row drivers and thus degrade the write pulse amplitude. The voltage gradient was eliminated by providing more N⁺ contacts on subsequent wafer runs.

Wafer Run C30

This wafer run had characteristics similar to C26 and C27 due to the voltage gradient.

Wafer Runs C35, C36, C37

Each of these runs had approximately 100 good dice. Dice from C35 and C37 had the best retention characteristics and were used for prototype evaluation. The $\phi 2$ circuit was found to have a current path in the non-select mode which caused a chip power dissipation of 200 mw. Two mask changes were made to improve the circuit.

Wafer Runs C41, C42

Each of these runs had approximately 60 good dice. Dice from these runs were used to populate the two deliverable prototype hybrid modules. The mask change to reduce the leakage path in the $\phi 2$ circuit caused a reliability problem with $\phi 1$ kept in a negative voltage state when the part is in a non-select mode. One logic condition added to the $\phi 2$ control will be implemented for any subsequent processing.

3.8 Beam Lead

Under the subject contract, the Sperry Univac beam lead development approach had a specific constraint applied which dictated that the basic MNOS process would not be modified since any wafer process modification might have serious technical liabilities. A proven MNOS process was assumed with no further process development except to optimize basic chip performance. The beam lead process would be considered to be additional processing steps independent of the MNOS processing. The major implication was that the aluminum interconnect metal on chip would remain. Gold is the metal most widely used to make the actual beam leads. In order to facilitate the processing of the gold beam leads, a refractory metal interface between the gold and aluminum was selected to prevent the known formation of gold/aluminum intermetallics. Alternative approaches were analyzed and an approach was taken which used a titanium tungsten interface.

An initial development of the beam lead process for the SU200 was carried out on the special designed TE101 test chip. The test chip had a fixed and memory transistor source/drain, gate, and substrate connections brought out to a beam lead bond pad and a ball and wire bond pad in order to facilitate electrical testing of the transistors and measurement of the transistors and measurement of the resistance of the gold to aluminum interface. Several wafers received the beam lead sputtering steps. Experiments for beam lead buildup, metal etching, and electrical characteristics were performed. The results of the investigation are summarized as follows:

- a) Varian, an outside vendor, reported no difficulties in sputter-cleaning and sputter-deposition of tungsten-titanium on the exposed aluminum pads of the TE101 test wafers, nor with gold sputtering over the W-Ti.
- b) The gold-plating and stripping solutions attacked the aluminum beam lead bonding pads on TE101 test wafers, and that all coatings on the wafer - sputtered gold and tungsten-titanium, and SiO₂ glassivation - were porous; i.e., areas of the wafer not protected with photoresist permitted the passage of plating or stripping solutions through the coatings down to the silicon substrate with destruction of aluminum metallization.
- c) Scanning electron micrographs shown the glassivation layer to have a porous surface.
- d) Electrical tests on the test transistors indicated that the memory transistors operated properly after sputtering, but the fixed transistors exhibited a threshold shift. It was found that the threshold shift could be partially annealed out. The electrical resistance of the gold/aluminum beam lead interface was low.

The investigation to beam lead aluminum bond pads with gold pointed out several steps in the process which require further development. Also, the overall technical feasibility of beam leading an MOS device with an aluminum metal interconnect is not proven and may not be realistic. The trade-off between beam lead development and cost, schedule, quantity of deliverable parts and technical risk led to the deletion of the beam lead requirement from the SOW. The SU200 was laid out with bond pads in a beam lead pattern which can directly facilitate add-on beam lead processing at a later date if an adequate beam lead process is developed.

3.9 Device Assembly

The SU200 die were individually packaged in 40-pin Dual-In-Line packages. The following packaging steps were used:

- a) The wafers are gold-backed to provide a reliable bonding surface.
- b) A diamond impregnated dicing wheel used to cut 3/4 of the way through the wafers.
- c) The dice are separated through the use of a breakmaster wafer breaker.
- d) Gold eutectic bonding is used to secure the die to the package.
- e) Ultrasonic gold ball bonds are used to electrically connect the die to the package pins.
- f) A gold-plated Kovar Lid is sealed with a 80/20 Gold Tin solder pre-form.

3.10 Test Requirements

The SU200 must meet the final contract Performance Specifications of Section 2.0. The critical conditions are 5000 hours of no power retention and 10^8 read cycles with a 6.0 μ s write and a 2.5 μ s read over the temperature range of -25° C to 70° C.

3.11 Prototype Chips

The deliverable requirements for prototype chips are 10 dice which have passed electrical probe, 10 DIP packaged devices which have passed SOW requirements, and 6 DIP packaged devices which have passed functional tests. Ten dice have been delivered which passed all pattern and pattern sensitivity tests at 25° C with a 2.5 μ s read and a 6.0 μ s write. Ten DIP packaged devices passed all pattern, pattern sensitivity tests and 10^8 read cycle retention tests at -25° C, 25° C, and 70° C while dissipating less than 800 milliwatts of power. Six DIP packaged devices passed pattern and pattern sensitivity tests over temperature. Twelve other DIP packaged devices were programmed at 25° C and have been tested periodically for data retention. Four of the devices received a 6 μ s write, 4 devices received an 8 μ s write and 4 devices received a 10 μ s write. Each group of four devices had the following data patterns; ones, zeros, checkboard, and checkerboard not. All twelve devices have held data longer than 5000 hours. Four other DIP package devices have greater than 1500 hours of no power data storage at 70° C. The SU200 prototype DIP package devices have met all of the final SOW requirements except for verification of long term storage at temperature extremes; however, testing on monitor devices verifies the capability of the SU200 to meet 5000-hour no power storage requirements.

4.0 MIL-STD-883 Evaluation Testing

4.1 Summary

Ten deliverable and six functional SU200 40-pin DIP prototype devices were subjected to the test procedure illustrated in Figure 4.1. The specific test procedures and sample sizes are given in Table 4.1. The SU200 was found to have a fixed gate breakdown mechanism when operated continuously at high temperature. One of the ten devices failed during the temperature cycling. No determination of the failure mode could be made. Six of nine devices failed the 70°C burn-in for 160 hours. Four of the six failed devices were analyzed via microprobe after the die cover glass was removed. All devices had inoperative read power strobe circuits which indicated a fixed transistor failure. Four of the six functional reserve devices failed the 1000 hour operating life test at 70°C. Similar failure patterns were encountered on these devices. No mechanical failures or visual defects were encountered. The primary failure mechanism appeared to be the fixed gate breakdown.

4.2 Results

4.2.1 Screen Tests

Internal Visual

This test was performed on non-functional devices and no visual defects were found.

Stabilization Bake

The ten deliverable devices were subjected to the stabilization bake.

Temperature Cycle

The ten devices were subjected to the temperature cycle.

Acceleration

The ten devices were subjected to the 5000 G acceleration.

Hermetic Seal

The ten devices were subjected to both the fine leak and gross leak.

Electrical

Nine of the ten devices passed the 25° C electrical tests.

Burn-in

Three of the nine devices were subjected to continuous read/write cycling for the test period. One device failed and two devices passed electrical tests but had reduced retention of 10^8 read cycles to 10^6 read cycles. The remaining six devices were subjected to continuous read cycling for the test period. Four devices failed and two devices passed electrical tests but had reduced retention from 10^8 read cycles to 10^7 read cycles.

Electrical

The results were discussed in the burn-in section.

Electrical

The results at -25°C and +70°C were the same for the functional devices.

4.2.2 Quality Conformance

Electrical

Six back-up devices were tested and passed the electrical tests over temperature. However, the devices had less than 10^8 read cycle retention.

Operating Life

Four devices were subjected to continuous read/write cycling for the test period. The devices were tested periodically at 70°C for pattern sensitivity. Device 2 failed at 72 hours, device 3 failed at 768 hours, device 1 failed at 912 hours, and device 0 failed at 960 hours. None of the device operated for the full 1000 hours. Device 0 passed all pattern and pattern sensitivity tests at 25°C and had 3×10^4 read cycle retention. The other three devices had approximately 128 bit failures with the all 0's pattern and 8 bit failures with the all 1's pattern.

Temperature Cycle

The four devices from the operating life test were subjected to the temperature cycle test.

Acceleration

The four devices were subjected to the acceleration test.

Hermetic Seal

The four devices exhibited no leakage during the hermetic seal test.

Electrical

The four devices exhibited no change in electrical characteristics in comparison to results after the operational life test.

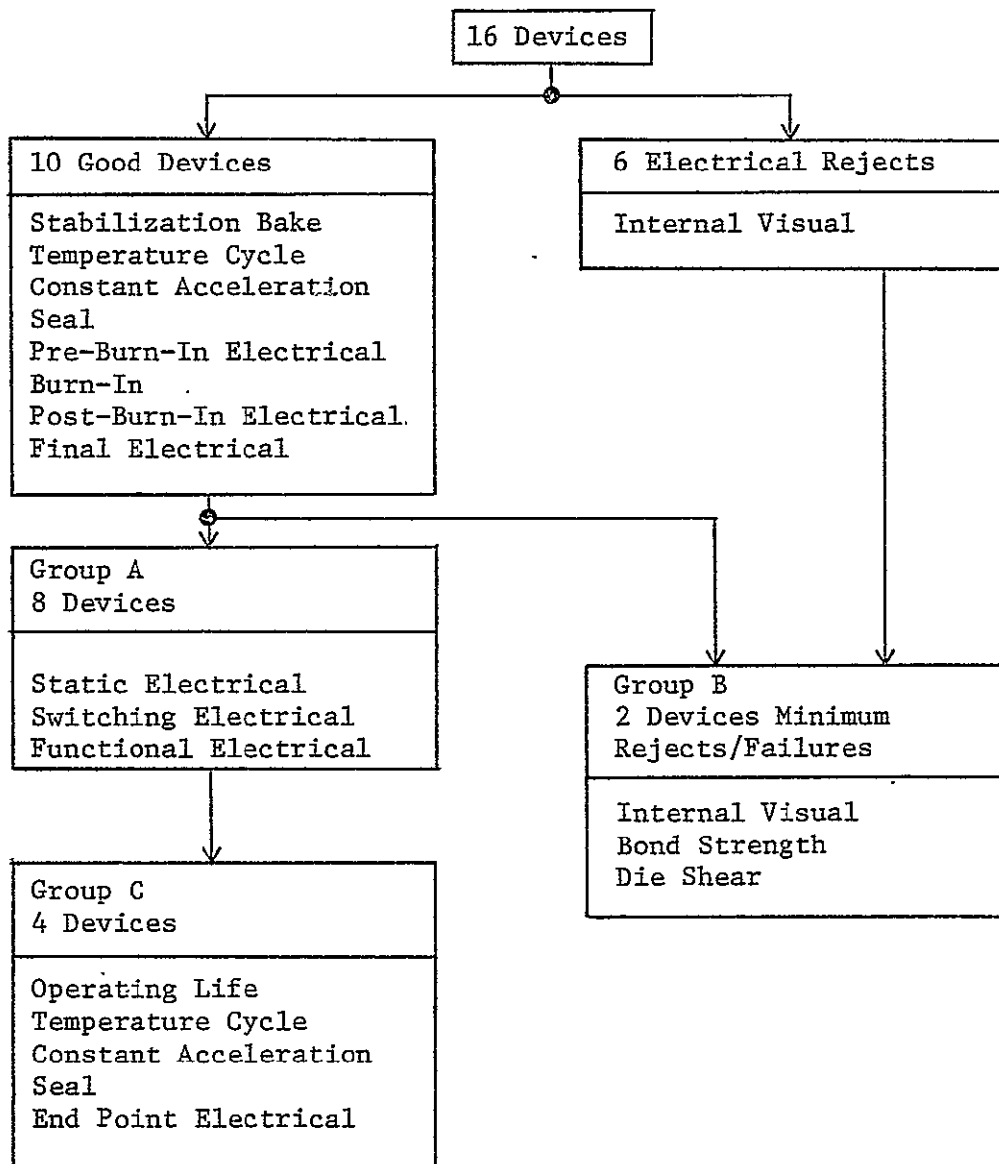


Figure 4.1. MIL-STD-883 Test Flow Diagram

Procedure	Sample Size	Number Failed
A. Screen Tests		
1. <u>Internal Visual</u> - Open the electrical reject devices and perform the inspection of Method 2010.1, Condition B.	6	0
2. <u>Stabilization Bake</u> - Subject the samples to a 24-hour minimum bake at +150°C per Method 1008, Condition C.	10	0
3. <u>Temperature Cycle</u> - Subject the devices to ten temperature cycles from -65°C to +150 C per Method 1010.2, Condition C.	10	0
4. <u>Acceleration</u> - Subject the devices to the 5000 G acceleration of 1 minute in the Y ₁ axis only per Method 2001.2, Condition E.	10	0
5. <u>Hermetic Seal</u> -		
a. <u>Fine Leak</u> - Test per Method 1014.2, Condition B. (Package Volume - 0.07 CC).	10	0
b. <u>Gross Leak</u> - Test per Method 1014.2, Condition C.	10	0
6. <u>Electrical</u> - Return the devices to the test engineer for electrical measurements at 25°C per the device specification.	10	1
7. <u>Burn-in</u> - Perform a dynamic burn-in at +70°C for 160 hours per Method 1015, Condition D. The test engineer shall define the test circuit.	9	6
8. <u>Electrical</u> - Return the devices to the test engineer for electrical measurements at 25°C per the device specification.	9	6
9. <u>Electrical</u> - Measure electrical parameters at -25 C and +70°C per the device specification.	9	6

Table 4.1 Test Procedures (Sheet 1 of 3)

Procedure	Sample Size	Number Failed
B. Quality Conformance		
1. <u>Electrical</u> - Measure the following parameters at -25°C, 25°C, and +70°C. a. Static (current drain, leakage) b. Switching c. Functional	8	0
2. <u>Operating Life</u> - a. Perform a dynamic operating life test for 1000 hours at +70°C per Method 1015, Condition D. The test engineer shall define the test circuit.	4	4
b. Return the units to the test engineer for point electrical tests.	4	4
3. <u>Temperature Cycle</u> - Subject the devices to ten temperature cycles from -65°C to +150°C per Method 1010.2, Condition C.	4	0
4. <u>Acceleration</u> - Subject the devices to the 5000 G acceleration of 1 minute in the Y ₁ axis only per Method 2001.2, Condition E.	4	0
5. <u>Hermetic Seal</u> - a. <u>Fine Leak</u> - Test per Method 1014.2, Condition B (Package Volume = 0.07 CC).	4	0
b. <u>Gross Leak</u> - Test per Method 1014.2, Condition C.	4	0
c. <u>Electrical</u> - Return the devices to the test engineer for end point electrical tests at 25°C.	4	0

Table 4.1. Test Procedures (Sheet 2 of 3)

Procedure	Sample Size	Number Failed
C. Destructive Review	2	
If available, use two failed pieces minimum from the screen tests or from the initial electrical of the quality conformance tests.		
1. <u>Internal Visual</u> - Verify the internal design and construction per Method 1014.	1	0
2. <u>Bond Pull</u> - Perform the bond pull test of Method 2011.2, Condition D. Record all pull values.	2	0
3. <u>Die Shear</u> - Perform the die shear test of Method 2019.1. Record the shear force and note the percentage of silicon remaining attached.	2	0

Table 4.1. Test Procedures (Sheet 3 of 3)

4.2.3 Destructive Review

Internal Visual

The device had no visual faults.

Bond Pull

The two devices met the requirements of the bond pull.

Die Shear

The two devices met the requirements of the die shear.

4.3 Analysis

All of the device failures except one occurred during the longer term tests, either burn-in or operating life. The failure mode of the single device could not be determined. The other devices exhibited catastrophic failures in which all bits of a specific data pattern were bad or some multiple of 128 bits failed, such as 1024 bits. These types of failures are attributable to the control circuitry rather than the memory array in which single failures predominate.

SEM analysis was performed on the four devices which failed the continuous read during burn-in. All possible defects found under microscopic examination were photographed via SEM at high magnification. Only one device had a defect which could cause device failure while no processing type faults such as pin-holes or metal shorts could be attributed as causes for failure on the other three devices. The cover glass was then removed from the four devices and the internal circuits were probed. The read power strobe circuit was found to be inoperative in each case. The circuit layout and circuit schematics were checked once again with no layout rule violations found and no logical errors found. Since the layout was found to be correct, the device failures appeared to be process related and accelerated by continuous operation at high temperature.

Since the failure mode was caused by continuous operation, several fixed gate test transistors on a wafer from run C35 and a wafer from run C37 were subjected to continuous positive and negative 30-volt gate pulses. The wafer from C35 had more gate failures than the C37 wafer which correlates well with the fact that wafer run C37 produced more dice with good characteristics. The integrity of the gate oxide is the probable cause of the SU200 failures. Another more recent MNOS part has exhibited similar gate breakdown problems which were solved by making the gate oxide thicker and by improving the oxide growth process. Similar techniques are applicable to the SU200 process but were not part of these runs.

The reduction of the retention capability of the memory gates due to repeated write cycles and to a lesser extent with repeated read cycles is a characteris-

tic of nitride gates. The retention/write cycle dependence is process dependent and can be optimized by varying nitride thickness, composition, and deposition temperatures. Also a Low Pressure Chemical Vapor Deposition Technique has been developed for nitride which improves write characteristics and surface uniformity. This technique can also be applied to the SU200.

5.0 Hybrid Module Development

5.1 General

This task required the development of a hybrid memory module organized as 2048 words by 8 bits which utilized the 2048 bit SU200. The module was designed with sufficient control to be used in higher order systems. The hybrid module development tasks are summarized in Figure 5.1.

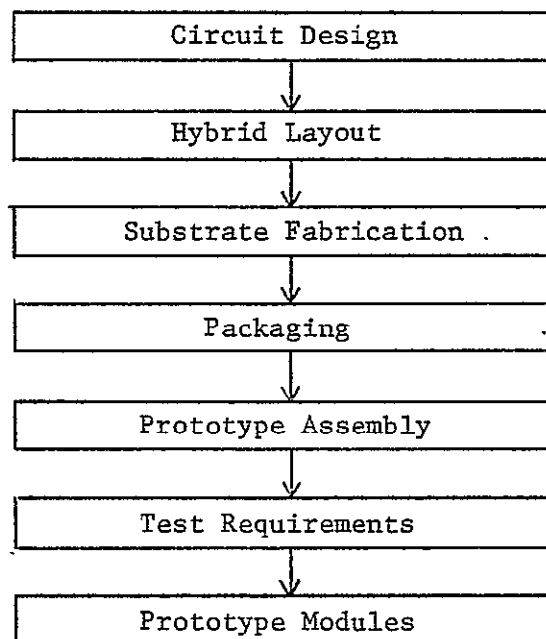


Figure 5.1. Hybrid Module Development Tasks

5.2 Circuit Design

A hybrid module design was mutually agreed upon by NASA and Sperry Univac personnel which would have eight SU 200 memory chips organized as 2048 words by 8 bits. Six CMOS interface chips are used to buffer the SU200 CMOS level input and output signals on and off the hybrid module. Separate PMOS Power Strobe (PS) signals are brought directly onto the hybrid module for each SU200 along with a common $\phi 1$ PMOS signal (Figure 5.2).

5.3 Hybrid Layout

The hybrid module is two inches square with 30 pins on each of two sides of which 42 pins are used. A three-level metal interconnect was used for the substrate layout. The layout minimized capacitance between metal layers which crossed or ran parallel and also had no metal lines under the die except for voltage pads for substrate connections. The layout provided for sufficient current bussing capability and heat dissipation. Figure 5.3 illustrates the hybrid module signal pins.

5.4 Substrate Fabrication

Ten hybrid substrates were fabricated initially to provide for engineering and prototype modules.

5.5 Packaging

Ball and wire bonds were used to make electrical connections to the SU200 and CMOS dice. The dice were attached with electrically conductive epoxy.

5.6 Prototype Assembly

A total of six hybrid modules were fabricated. Hybrids 1 and 2 were fabricated with SU200 dice from Wafer Runs 35 and 36, hybrids 3 and 4 were fabricated from Wafer Run 41, and hybrids 5 and 6 were fabricated from Wafer Run 42.

5.7 Test Requirements

The SU200 dice were screened at the wafer level for patterns, pattern sensitivity, and continuous read retention at 25°C. The dice were tested to 5×10^6 read cycles. The hybrid modules were tested at 25°C for patterns, pattern sensitivity and continuous read retention with a 3.0 μ s Read cycle and an 8.0 μ s Write cycle.

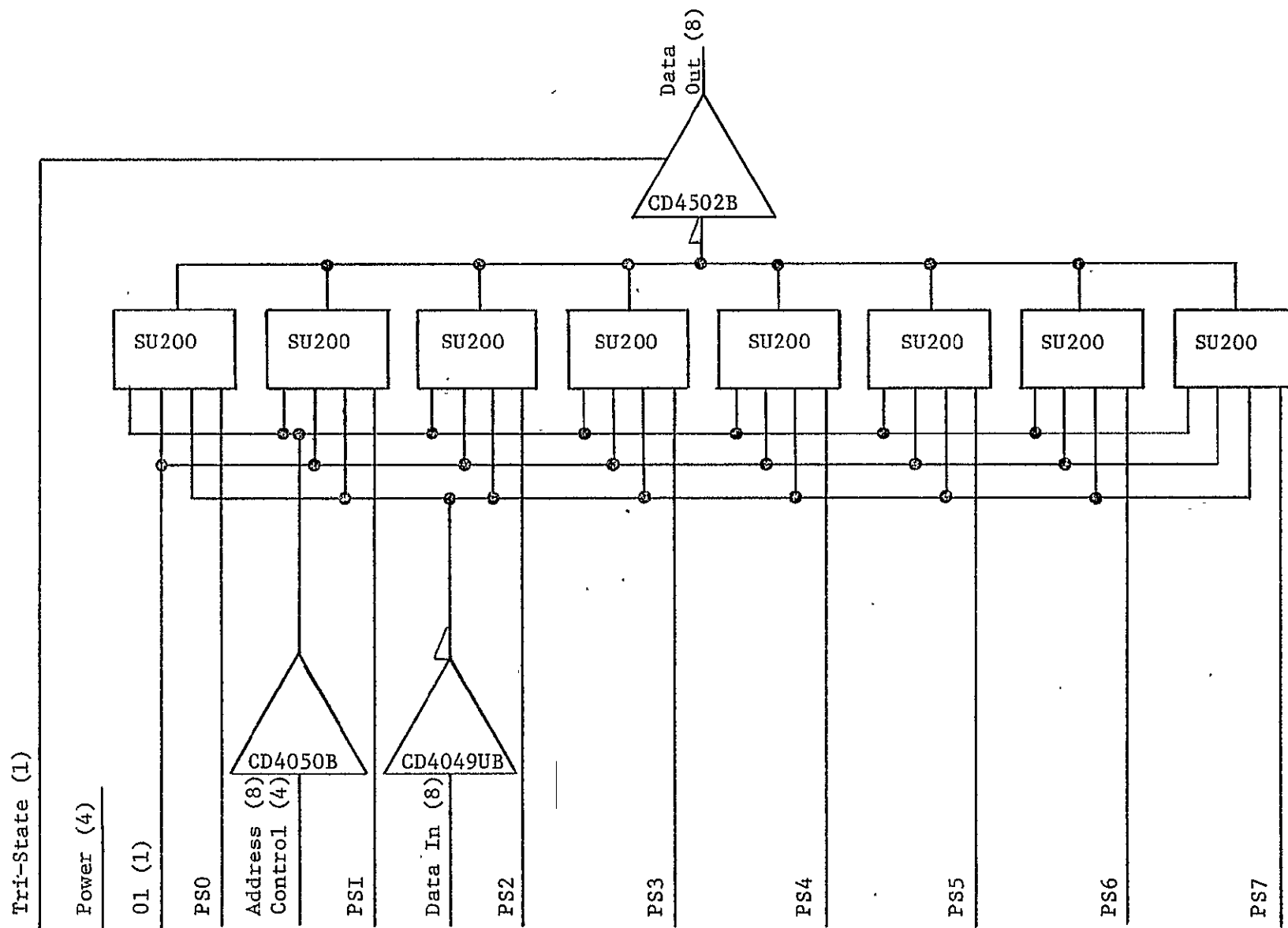


Figure 5.2. Hybrid Module Logic Diagram

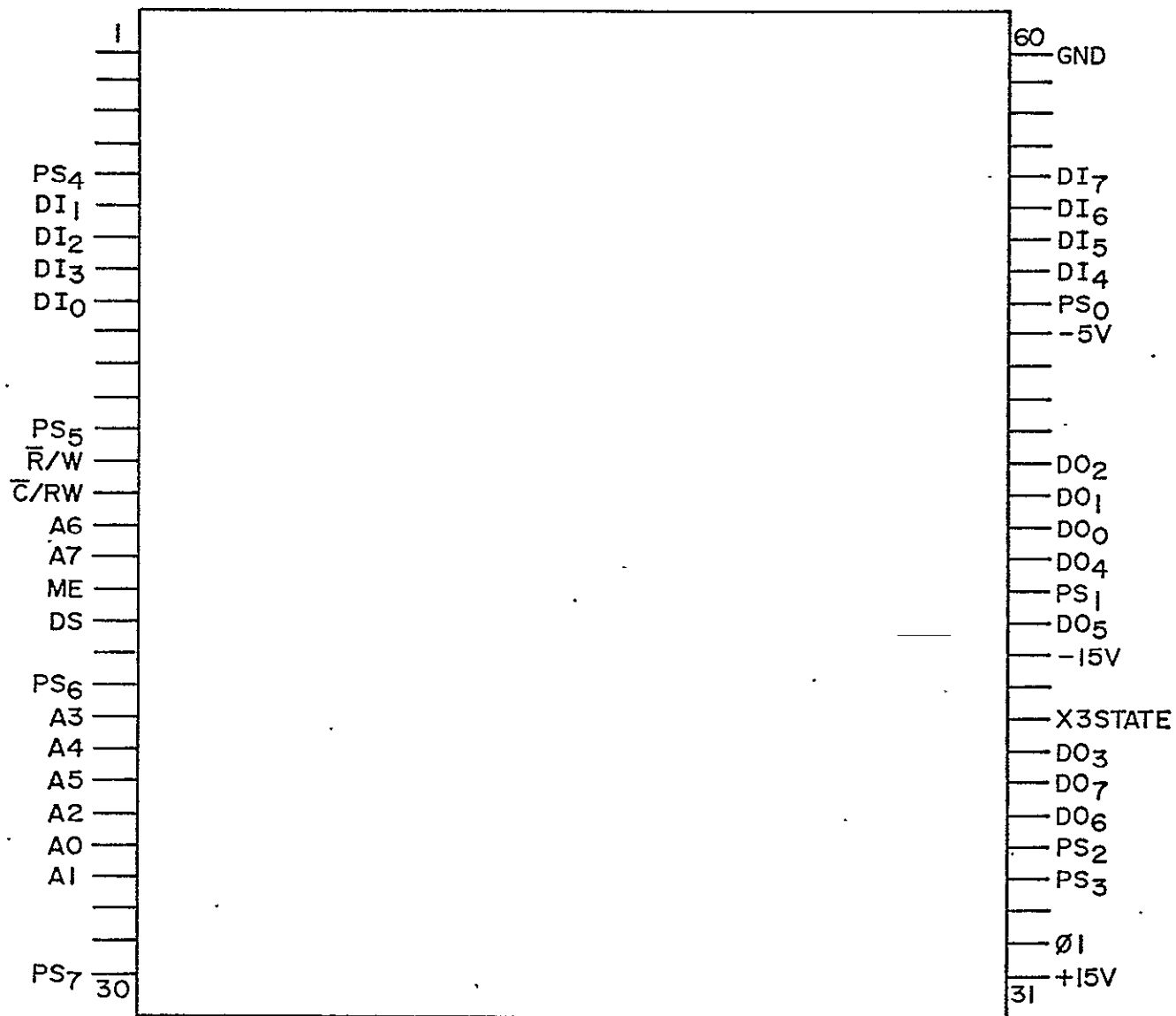


FIGURE 5.3 HYBRID MODULE

5.8 Prototype Modules

A total of six hybrid modules were fabricated in order to obtain two fully functional modules with good retention characteristics. Hybrid modules #1 and #2 were fabricated first and were found to be functional during electrical test. The hybrid design and concept of packaging eight SU200 devices in a single hybrid package were thus shown to be feasible. Hybrid #1 passed pattern tests but had low retention and was delivered with a clear cover for demonstration purposes. Module #2 passed all pattern and pattern sensitivity tests at 25°C. Current measurements on module #2 indicated current flow in the non-select mode of operation. The effect in the hybrid was that the seven unselected dice in the hybrid could each dissipate 200 milliwatts of power.

A design change was implemented and two more wafer runs, C41 and C42, were processed. The design change made was to leave $\phi 1$ at -10 volts in the non-select state and force the read circuitry to a low power state. Hybrid modules #3 and #4 were fabricated with dice from C41. The circuit change eliminated the current path, however the fixed gate breakdown of the transistors encountered in the DIP package evaluation was aggravated in the transistors gated by $\phi 1$. Several dice failures were encountered in modules #3 and #4 during operation with $\phi 1$ active in the non-selected state.

Hybrid modules #5 and #6 were fabricated with dice from run C42. The two modules were tested with $\phi 1$ in an inactive state in the non-select mode. Module #5 passed all pattern and pattern sensitivity tests at 25°C. The weakest SU200 die on the module had a continuous read retention of 0.9×10^7 read cycles before data loss. Module #5 had the most reliability of the modules tested. All of the dice on module #5 were from the same wafer which indicates that the wafer had overall good characteristics. Hybrid module #6 passed all pattern and pattern sensitivity tests at 25°C. The module was then tested for retention at 70°C to determine high temperature retention, however several SU200 dice failures were encountered. The dice failures in the hybrid can be attributed to the excess heat generated by the unselected dice and to the fixed gate breakdown under continuous operation at high temperature.

The inclusion of one logic condition on the $\phi 2$ buffer will eliminate the non-select current path in the SU200 device. Improvement of fixed gate process steps is discussed in the conclusions section 8.0. Testing was not performed at temperature extremes on the deliverable hybrids in order to ensure functional parts. No difficulty was experienced in the actual fabrication nor in the replacement of failed dice. The modules will be more difficult to repair with sealed covers. The hybrid module had no problems with pattern and pattern sensitivity tests and with proper screening of the SU200 dice will have good retention. Hybrid modules #2 and #5 were delivered.

6.0 Memory Exerciser

6.1 Description

The Memory Exerciser uses an Intel SBC 80/20 Single Board Computer as its controlling element. The SBC 80/20 includes an 8080A CPU, 2 K bytes of RAM memory, sockets for 4 K bytes of EPROM memory, full multi-master bus arbitrator logic which allows up to 16 CPU or controller masters to share the SBC 80 system bus, full programmable multimode eight-level vectored interrupt, two programmable interval times which may be used as real time clocks or for controlled I/O timing, 48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators and a programmable synchronous/asynchronous communications interface with RS 232C compatibility. A teletype adaptor which converts the RS 232C signals to a 20 MA current loop interface for use with a teletype. Baud rates for the communications interface are software programmable. A comprehensive system monitor residing in the two Intel 8708 EPROMs is in the system to facilitate the loading execution or debug of any new system software. Monitor commands include the ability to read and write hexadecimal paper tapes, execute pre-defined program segments, execute single program instructions, display move and alter memory contests, display and alter CPU register contents and read or write memory contests from or to paper tape. Monitor commands and resulting information may be initiated and displayed using a teletype or CRT terminal.

6.2 Design

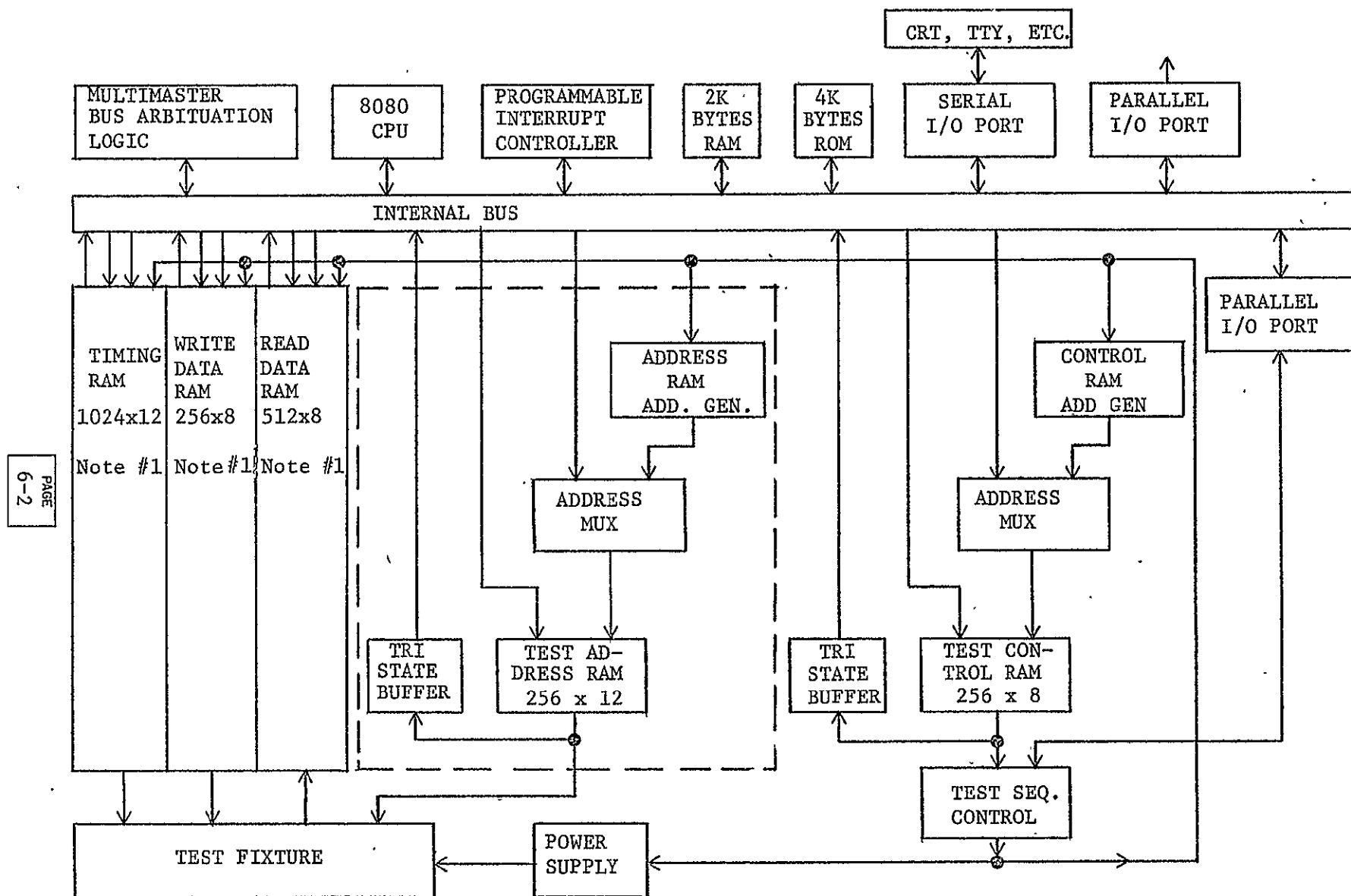
A block diagram of the system is shown in Figure 6.1. The system is organized so the Timing, Data Generator Address Generator and Test Control are portions of the processor memory located at memory addresses 4000-4FFF (Hexadecimal). When in the Test mode this portion of the memory is not accessible by the processor.

When not in the Test mode this portion of the memory may be used as required by the processor.

The following is a brief description of each of the sections of the exerciser as shown in Figure 6.1.

Timing

The timing section generates the pulses required to write data into and read data from the SU200. The 1024 x 12 Timing RAM is divided into two 512 x 12 sections, one for the Write cycle and one for the Read cycle. The technique used to generate the pulse patterns is to assign each pulse required to one bit of the 12-bit word. The RAM is then loaded with the information required to generate the desired pulse at the Device Under Test (DUT). For



NOTE #1. Configuration is similar to Test Address RAM (Blocks inside dashed box)

Figure 6-1. Memory Exerciser Block Diagram

example, if data in bit 0 of the RAM is loaded with a sequence of alternating 0's and 1's, as the RAM is sequentially addressed in the Test mode, the alternating 1's and 0's will be applied to the device pin assigned to bit 0.

The time that the data from each Timing RAM address is applied to the DUT is determined by the Timing RAM address generator. The timing address generator is a 9-bit binary counter clocked by a crystal controlled clock generator. The clock generator has four selectable output frequencies: 20 MHz, 10 MHz, 1.0 MHz and 0.1 MHz. These frequencies are selected by bits 8, 9 and 10 of the Timing RAM. The Timing RAM is capable of generating test cycles which range from 200 nsec to 5.12 μ sec in length.

Write Data RAM

The data to be applied to the DUT is generated in the processor and stored in the 256 x 8 Write Data RAM. When the system is in the Test mode the Write Data RAM is incremented by the Test control section of the system. During a Read operation the Write Data RAM is used for comparison to the data read from the DUT.

Read Data RAM

The Read Data RAM is used to store the data read from the DUT. The procedure used in the Exerciser is to read the data from the DUT, store it in the Read Data RAM, then evaluate the data after all the selected addresses have been read. This is done to more closely simulate actual system operation. The Read Data RAM has 512 addresses because some of the test sequences to test the disturb, address decoding and cross talk characteristics require more than one read at each address.

Address RAM

The address sequence applied to the DUT during the write or read test sequences is generated in the processor and stored in the 256 x 12 Address RAM. The addresses are applied to the DUT by incrementing the Address RAM's address generator via the Test Control section of the system.

6.3 Fabrication

The Memory Exerciser is a self-contained unit with all power supplies, microprocessor, interface circuitry and control circuitry. The actual fabrication was completed in a short period of time with no major design errors found during checkout.

6.4 Software

The hardware ROM section of the Memory Exerciser was expanded so that all control software is resident in ROM, thus no back storage devices are needed. The software for test sequences can be modified manually in the exerciser or special purpose routines can be entered via the RS 232 interface in order to expand the capability of the resident software package.

6.5 Test Control

All of the functions required to execute a test sequence are controlled by instructions which reside in the Test Control RAM. These instructions are entered into the memory via the Serial I/O port. In addition, a ROM located in the Test Control logic contains several blocks of instructions formatted to execute a specified test sequence. A block may be selected via the Serial I/O port and transferred into the Test Control RAM. Once the selected sequence is entered into the Test Control RAM, a Test Command is sent to the control logic. Once this is done, the system will execute the instructions in the Test Control RAM. When the instruction sequence is completed, the Test Control sends an Interrupt to the processor signifying completion of the test sequence.

6.6 Test Fixture

The system will have two Test Fixtures, one for testing packaged devices and one for testing a 2048 x 8 bit hybrid module. The fixture to test the packaged device will test or exercise eight devices serially or parallel, with the mode being selectable via the processor. When in the serial mode the device being tested is addressed by bits 8, 9, and 10 of the address word sent from the Address RAM. The fixture contains all the necessary high voltage drivers required to perform the testing on the packaged devices. In addition, provision has been made for a connector to route the test signals to a probe card if testing at the wafer level is required.

6.7 Documentation

The Memory Exerciser has a full set of documentation which will be delivered along with the exerciser. The documentation includes a full description of the hardware and software options, operating procedures, and engineering drawing.

7.0 Summary

7.1 Performance Specifications

The SU200 met the final SOW requirements of a 2.5 us read access time, a 6.0 us write time, an 800 mw maximum power dissipation, 10^8 read cycles before rewrite, 5000 hours of no power retention over the temperature range of -25°C to $+70^{\circ}\text{C}$. The SU200 requires four voltage levels of +15, 0, -4, and -10 volts. The control, input data and output data signal lines are CMOS compatible. Two PMOS level clock lines are used for chip selection and precharge.

7.2 Chip Development

The chip development effort involved the two major tasks of design and processing. The SU200 utilized a metal gate, p channel, MNOS process to achieve the requirement of non-volatile storage. The device requirement of 2048 bits of non-volatile storage was met with an organization of 256 words by 8 bits. A two transistor MNOS memory cell was used to facilitate differential sensing of threshold difference between the two transistors. The design phase was accomplished by the utilization of computer-aided circuit analysis of all circuit cells, the layout and interconnect of the circuit cells, and digitization and drive tape generation for mask making. The processing effort involved the optimization of several MNOS process steps to incorporate the constraints of high voltage levels inherent in the SU200 design. Source/drain breakdowns, oxide thicknesses, nitride compositions, and metal composition were improved. Several mask change iterations were made to the design to optimize process constraints and to incorporate design changes. The chip development effort resulted in a functional non-volatile semiconductor memory which met the final SOW requirement.

7.3 MIL-STD-883 Evaluation Testing

The ten SU200 devices which met the SOW requirements for the deliverables were used for the evaluation testing. The SU200 devices proved to have less than satisfactory reliability when subjected to burn-in and operational life testing at high temperature. Six of nine devices failed the 160 hour burn-in at 70°C and all 4 devices failed the 1000 hour operating life at 70°C . SEM analysis was performed on failed devices. Failure modes indicated that peripheral circuitry was at fault rather than the memory transistors. SEM analysis of surface faults proved to be inconclusive as to specific circuit failures. Four of the devices were microprobed and were found to have inoperative read power strobe circuits indicating fixed gate failure. Analysis of fixed gate test transistors identified a failure mechanism of gate breakdowns due to long term, high temperature operation. Similar observations have been made on other MNOS devices in which the gate oxides have been too thin. The problem of power dissipation in the non-select state was of no concern in the mode of continuous operation.

7.4 Hybrid Module Development

A hybrid design with eight SU200 devices and six CMOS devices in a single package was agreed upon by NASA and Sperry Univac to provide a package with an organization of 2048 words by 8 bits. The principal task was the layout and fabrication of the hybrid substrates. Six packages were assembled with a full complement of parts. Two hybrid packages passed all pattern and pattern sensitivity tests at 25°C while operating with a 3.0 μ s read access and 6.0 μ s write times. A high mortality rate was encountered in the SU200 devices when subjected to long term reliability testing which was previously encountered in the MIL-883 evaluation testing. Therefore, limited functional testing at high temperature was performed on the deliverable hybrid modules.

7.5 Memory Exerciser

A microprocessor controlled memory exerciser unit was designed, fabricated, and tested. The unit was used for the evaluation of both the DIP packaged SU200 devices and the hybrid modules. Flexibility was implemented in both the hardware and software to allow modifications to be made for the evaluation of other memory devices. Extensive pattern, pattern sensitivity and retention testing options were included in the exerciser design. The memory exerciser is an operational unit.

8.0 Conclusions

8.1 Performance Specifications

The SU200 deliverable devices met the final SOW operational requirement for speed, power, retention, interfacing, voltage levels and input protection. The SU200 is the densest and fastest true MNOS RAM presently available. The Non-Volatile Memory Development Program initiated by NASA was aggressive and the basic parameters have been met by the SU200.

8.2 Chip Development

The chip development effort demonstrated a chip design which met operational requirements and an MNOS process which provided the retention characteristics compatible with device speed constraints. The SU200 is not a mature device with respect to manufacturability. One design change to the $\phi 2$ buffer to eliminate standby power along with process optimization to improve overall yield reliability are necessary. The design change is minor while process improvements can be implemented based on an improved Sperry MNOS process. The basic SU200 process was conceived in 1976 and several process steps and process equipment have been improved and have evolved in the 3 year program period. Low Pressure Chemical Vapor Deposition (LPCVD) for nitride would be used on subsequent SU200 product, a new mask set would be generated to facilitate use with projection alignment, an optimized thermal gate oxide process would improve fixed gate breakdowns and an improved oxide etch technique would be used to eliminate possible metal cracking over contact steps.

8.3 MIL-STD-883 Evaluation Testing

The MIL-STD-883 testing was performed to evaluate the maturity and reliability of the SU200 device. The SU200 was found to have a failure mechanism of fixed gate breakdown when subjected to continuous operation at high temperature. One of ten devices failed during test after temperature cycling, six of nine devices failed the 160 hour burn-in at 70°C, and all four devices failed the 1000 hour 70°C operating life test. No mechanical failures or visual defects were found. Failure analysis indicated gate ruptures on the fixed gate devices due to thin oxides or oxide integrity. As indicated in section 8.2 several process steps could be improved to increase the device reliability and specifically for the fixed gates to increase the gate oxide thickness and optimize the thermal oxide in HCl atmosphere growth.

8.4 Hybrid Module Development

Two fully functional hybrid modules were fabricated which were populated with eight SU200 devices and six CMOS devices. The hybrid modules were susceptible to the failure mechanism encountered in the MIL-STD-883 testing. The hybrid modules can be manufactured; however, substantial prescreening is necessary at the wafer level to find dice with good retention characteristics.

9.0 Recommendations

9.1 Chip Design

The present chip design meets the final SOW requirements and with a minor circuit improvement is satisfactory. The SU200 design, however, utilizes only P channel enhancement devices and requires high voltage bootstrap circuits to sustain full internal voltage swing. Sperry Univac has an improved MNOS process which utilizes P channel depletion devices. The depletion devices eliminate the need for bootstrap circuits and reduce on chip voltages from 45 to 30 volts, thus provide a reliability improvement. The improved process has tighter layout design rules due to the lower voltages which would reduce the chip size to below 200 mils on a side, lower power consumption and improve circuit performance with the lower parasitic capacitances.

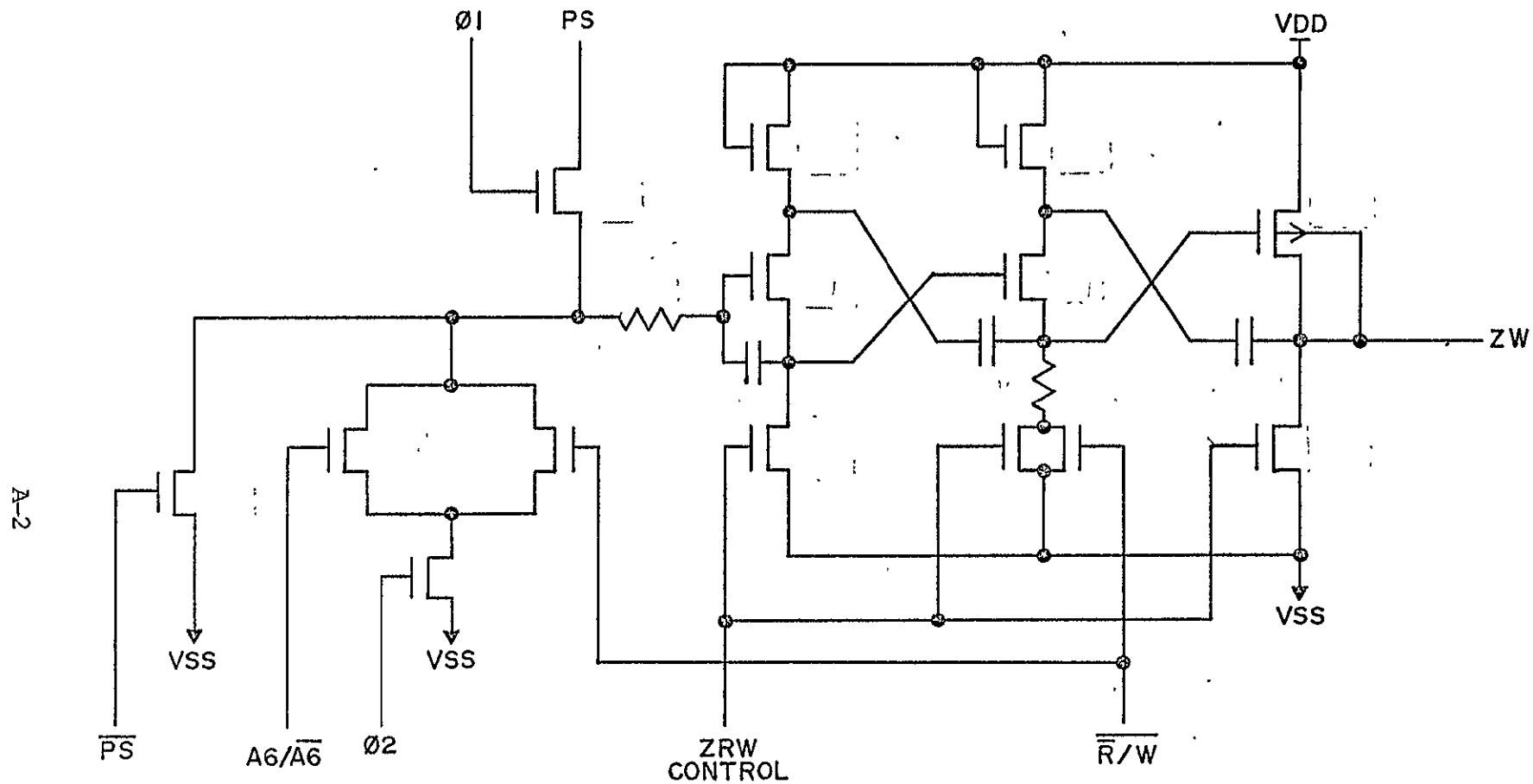
9.2 Chip Processing

The present SU200 MNOS process has been engineered to provide functional SU200 devices. The failure mechanism of the SU200 devices has been identified as a thin oxide in the fixed gate transistors. This type of a problem is addressed in the next effort of a chip development effort which is a manufacturing methods program to improve device yield. Device yields have been found to statistically improve with the amount of material processed. The SU200 has to be produced on a production basis in order to improve overall yield and improve reliability.

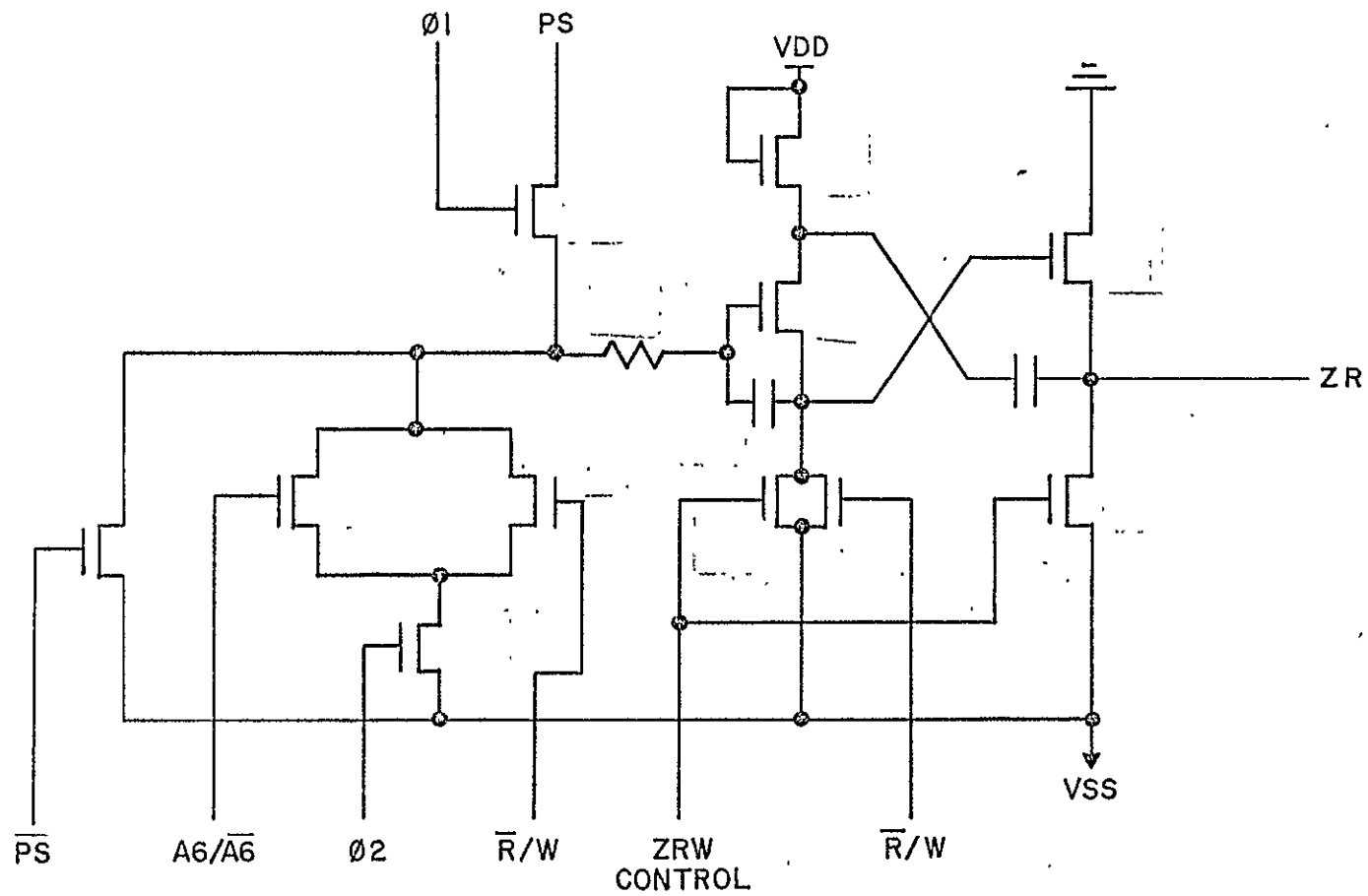
As mentioned in Section 9.1 Sperry Univac has an improved MNOS process which uses depletion load devices and may be an appropriate process for the SU200 is production quantities warrant a redesign. The improved process has along with implants for depletion loads and field inversion; Low Pressure Chemical Vapor Deposition (LPCVD) for nitrides which improve nitride consistency across a wafer and nitride programming characteristics; and thicker gate oxides grown with an improved Dry HCl process for higher gate breakdowns and low defect density.

APPENDIX A

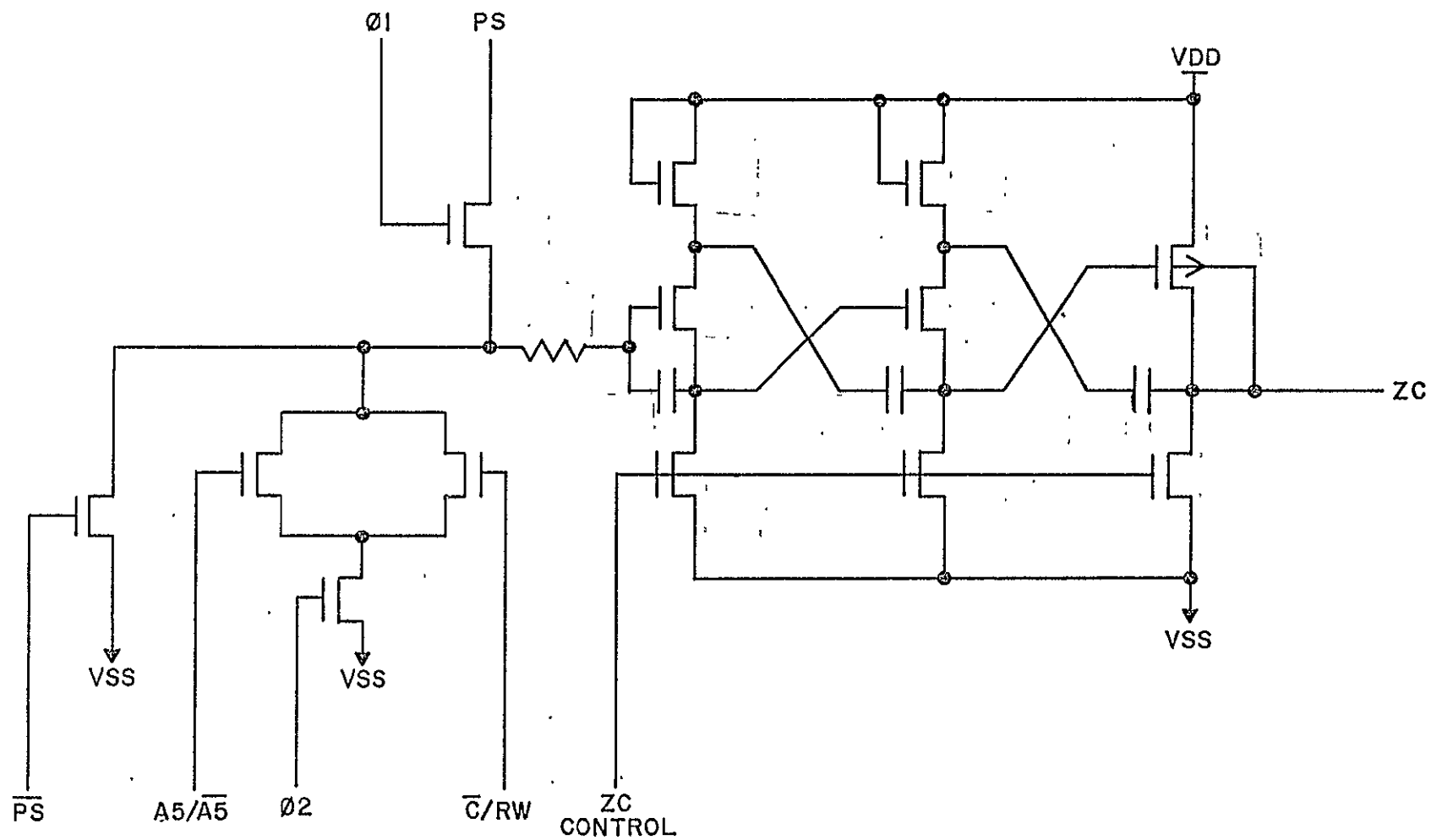
SU200 Circuit Schematics



NASA RAM
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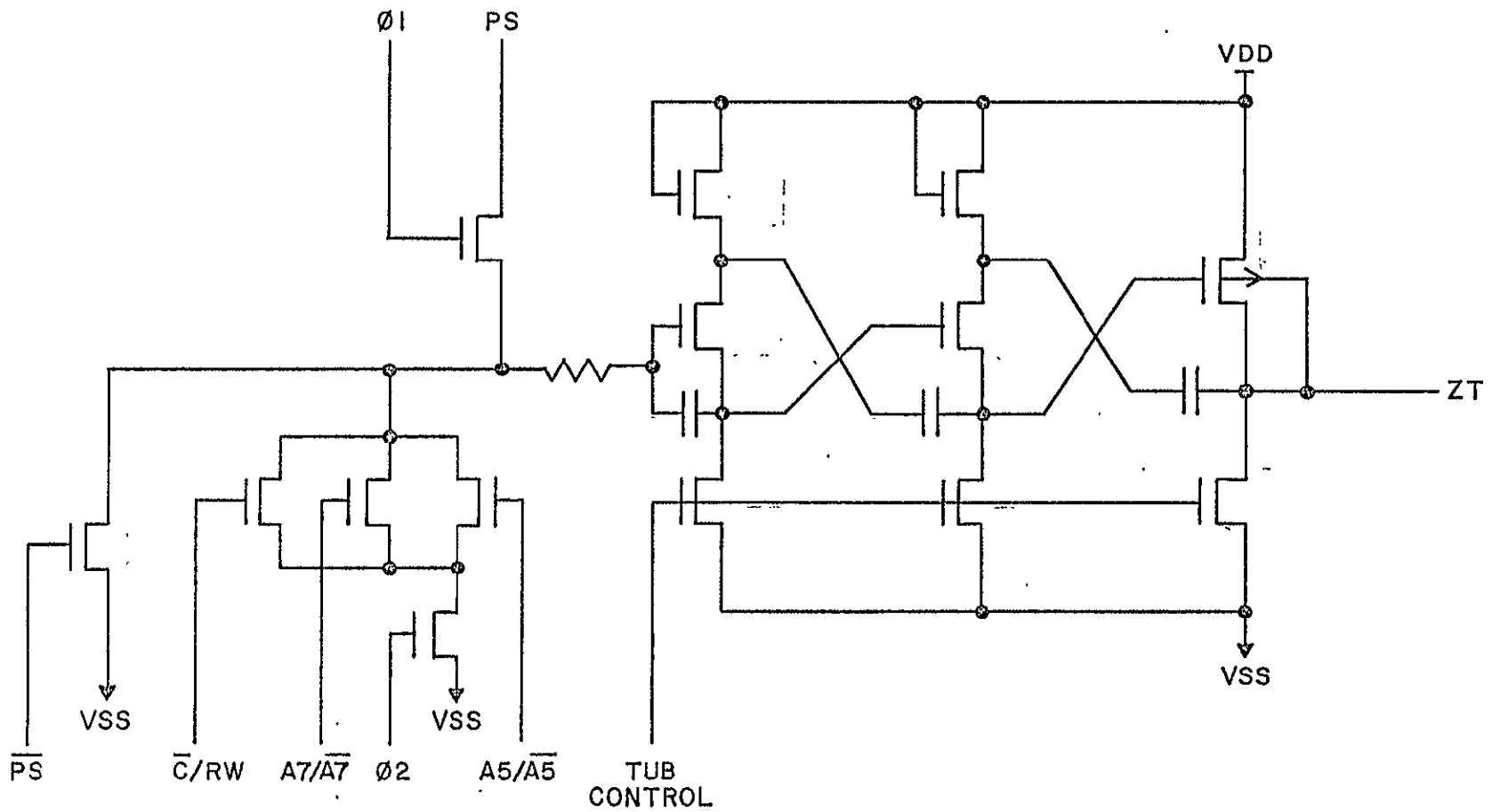


NASA RAM
READ SECTION OF Z_{RW} DRIVER

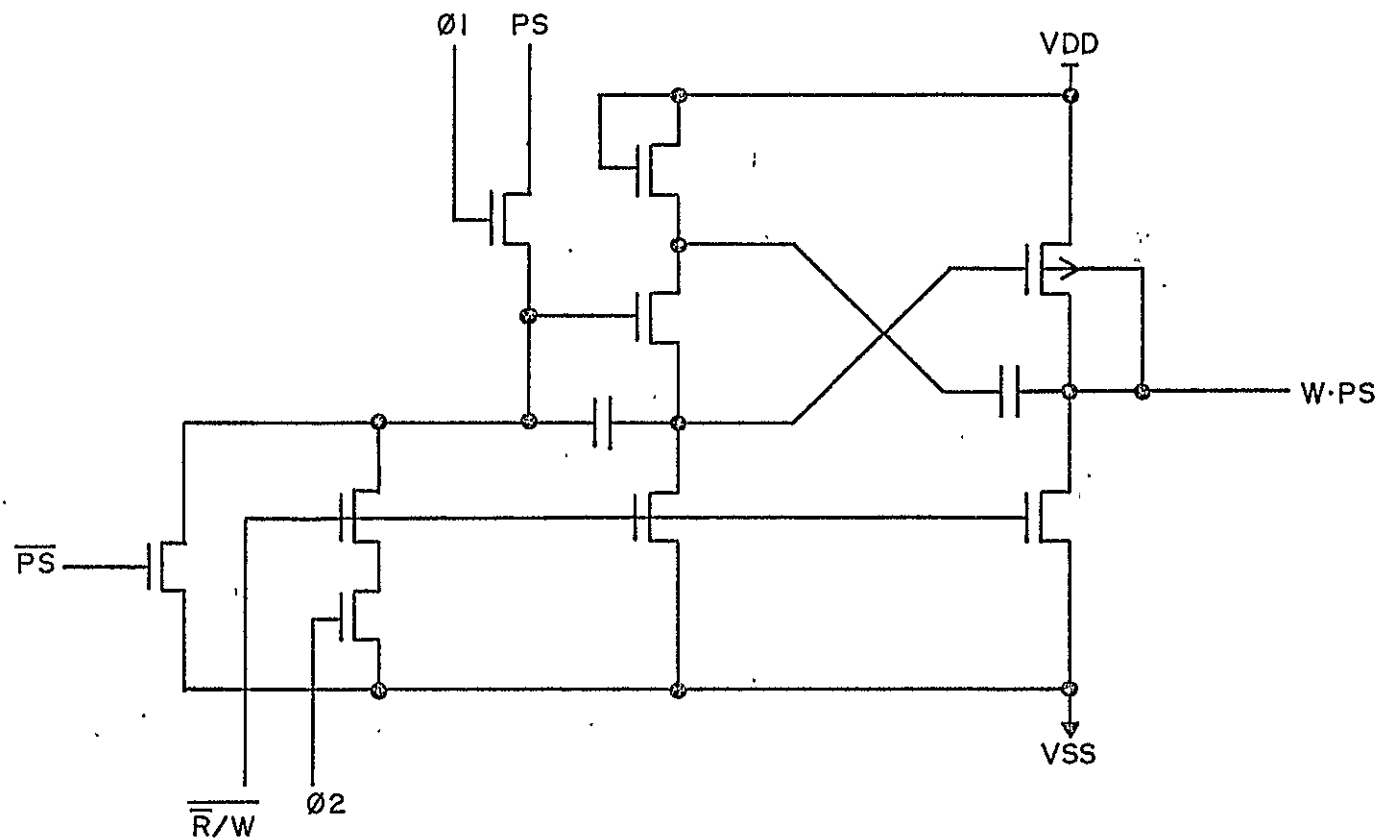


NASA RAM
ZC DRIVER

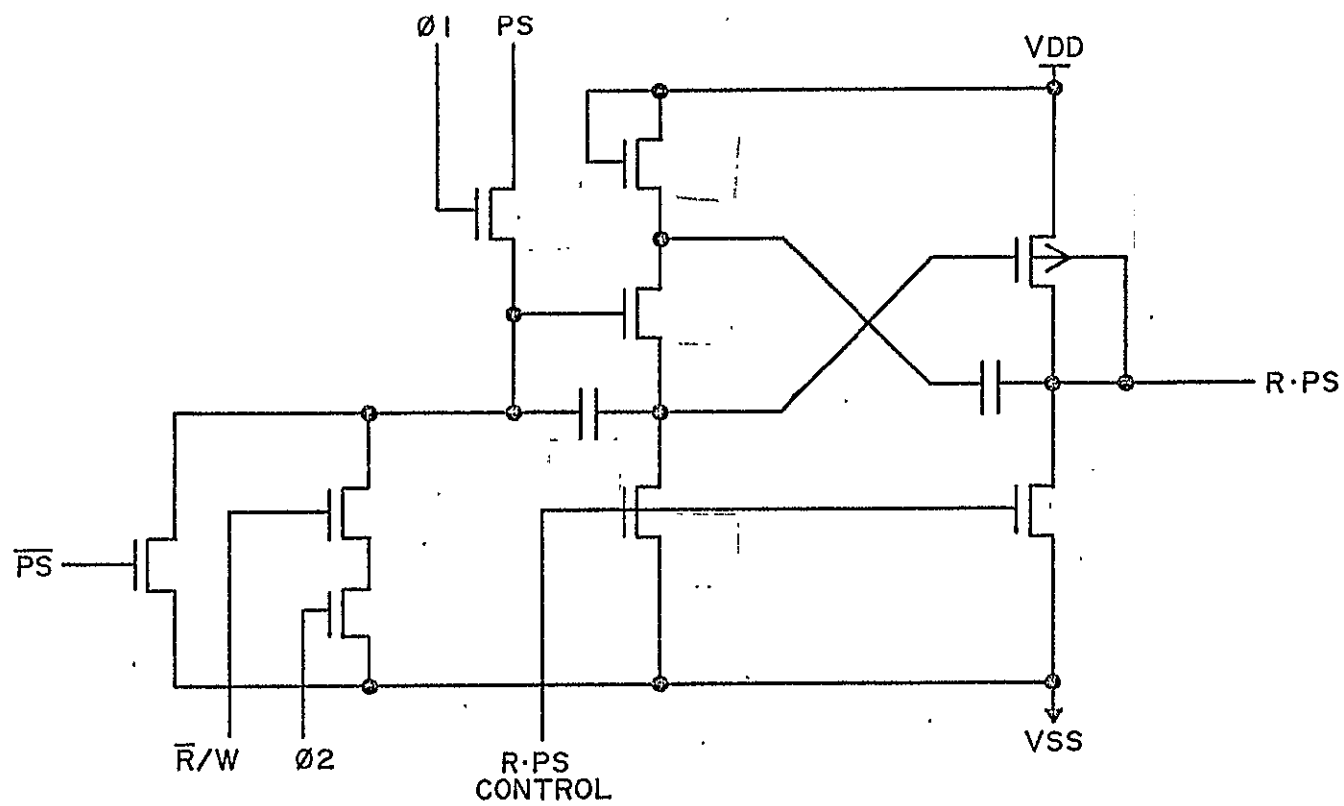
A-5



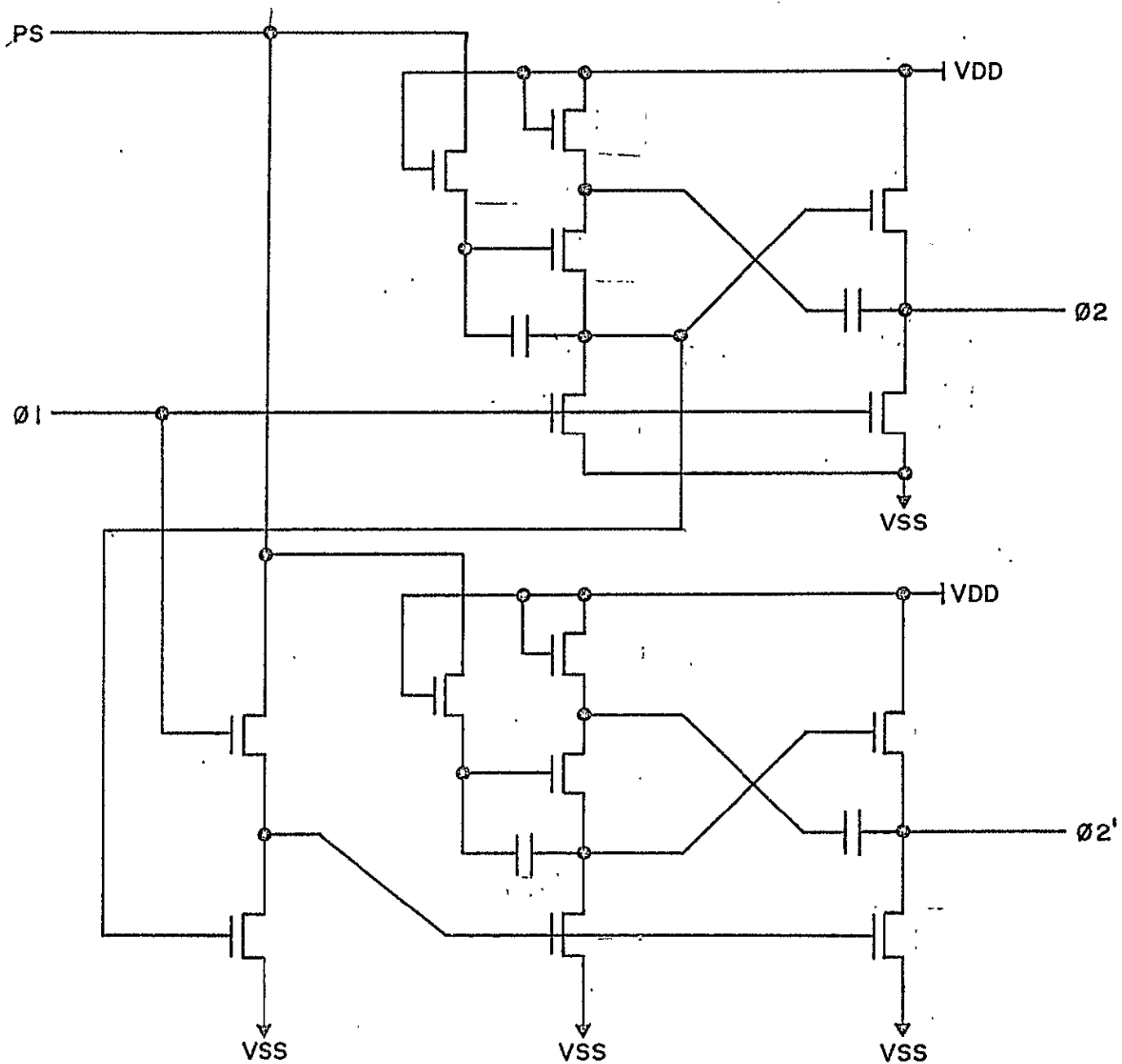
NASA RAM
TUB DRIVER



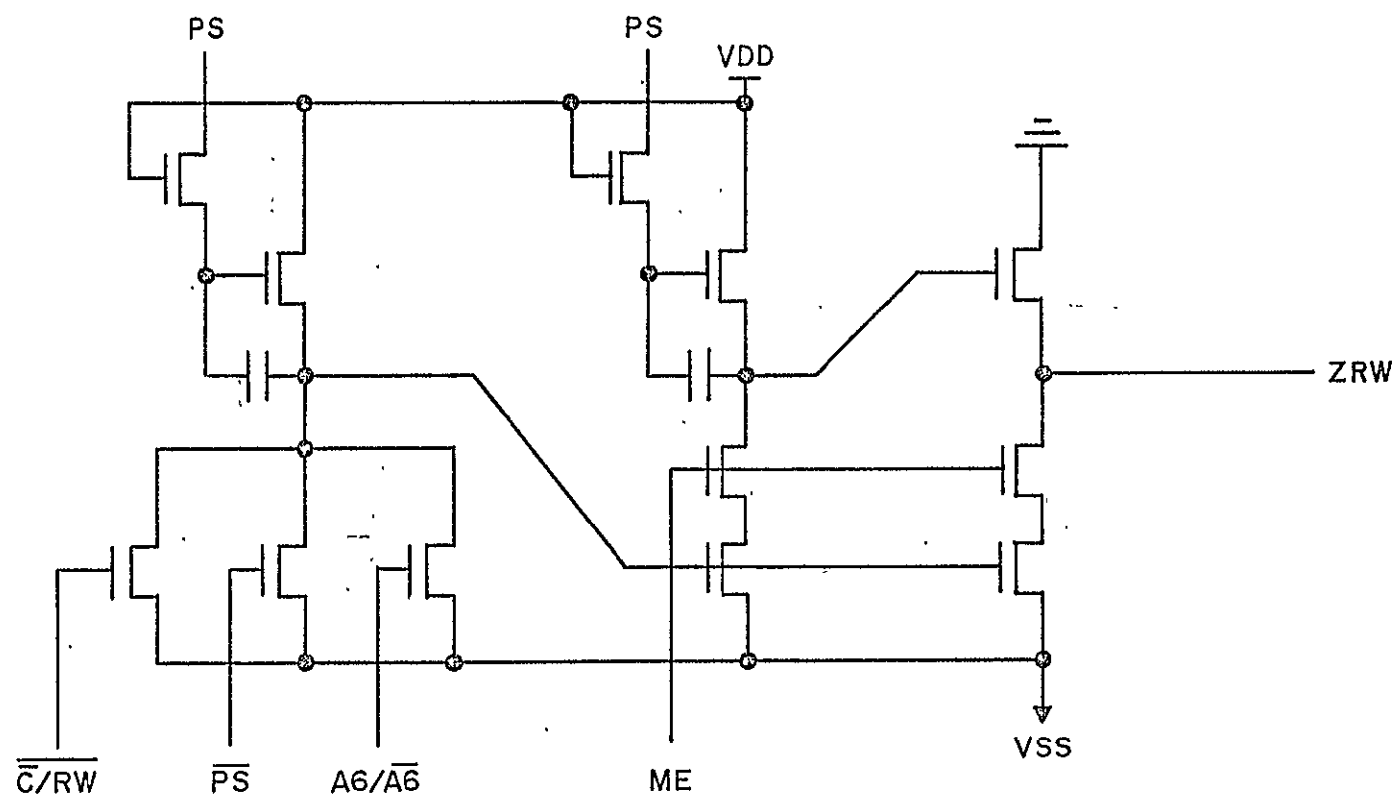
NASA RAM
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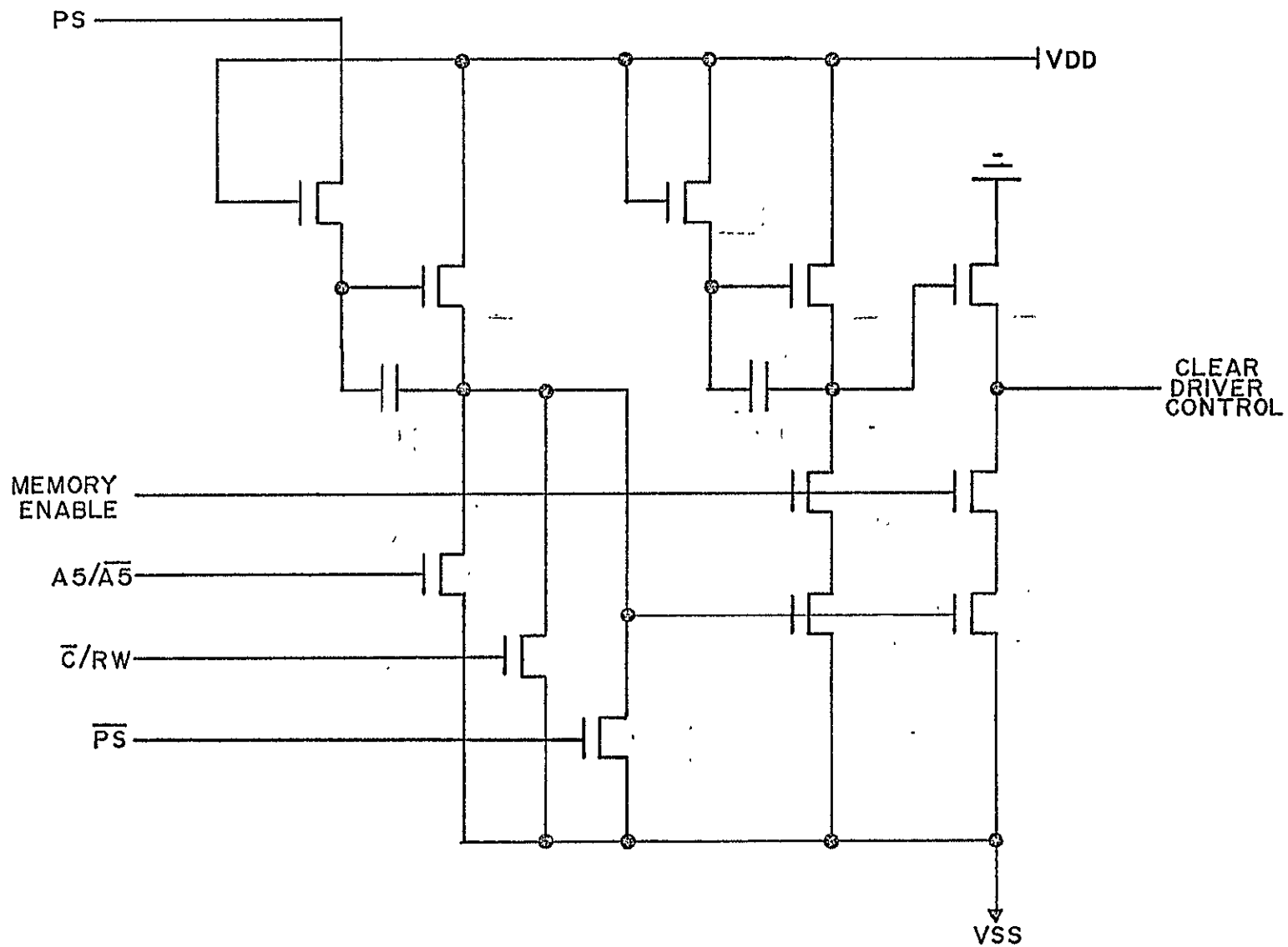
NASA RAM
READ POWER STROBE



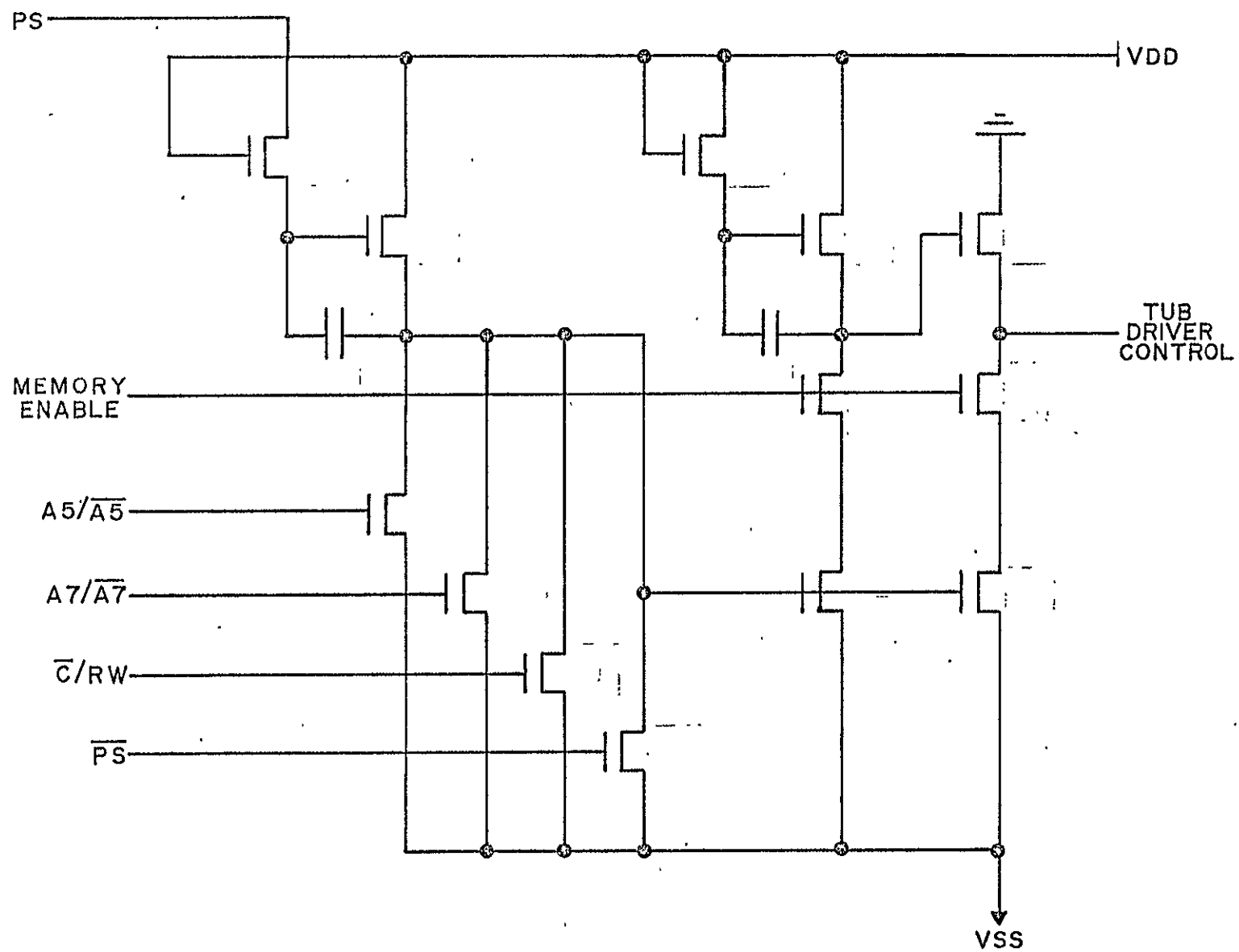
NASA RAM
Ø2 & Ø2' DRIVERS



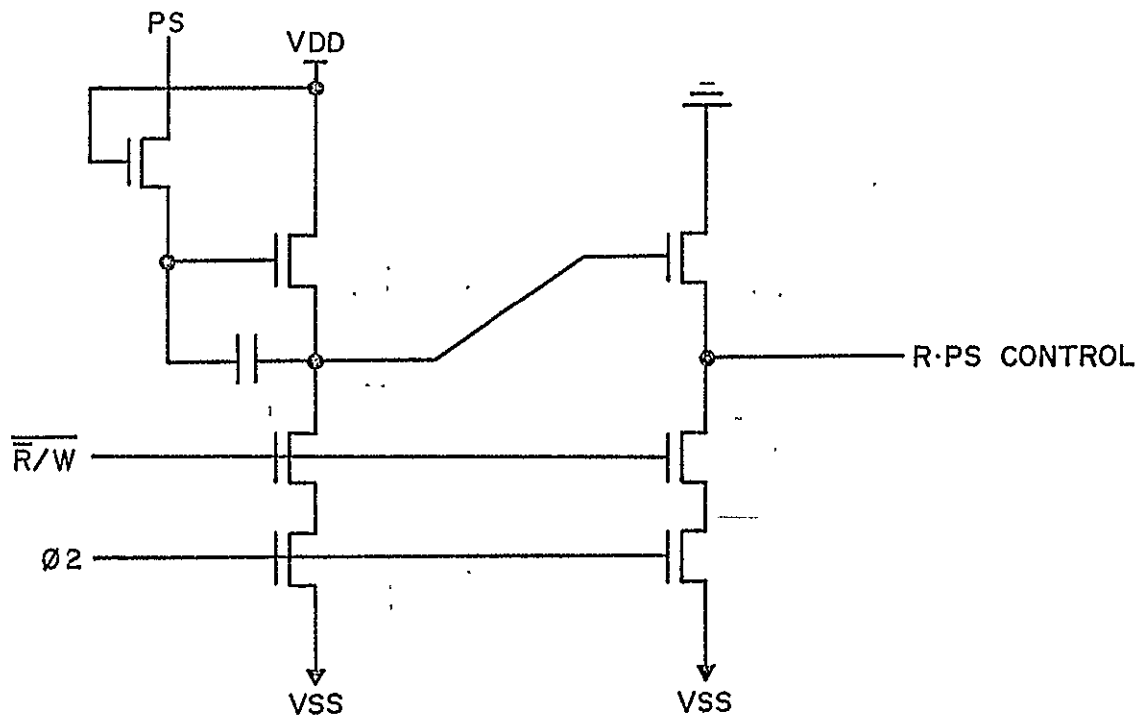
NASA RAM
CONTROL FOR Z_{RW} DRIVER



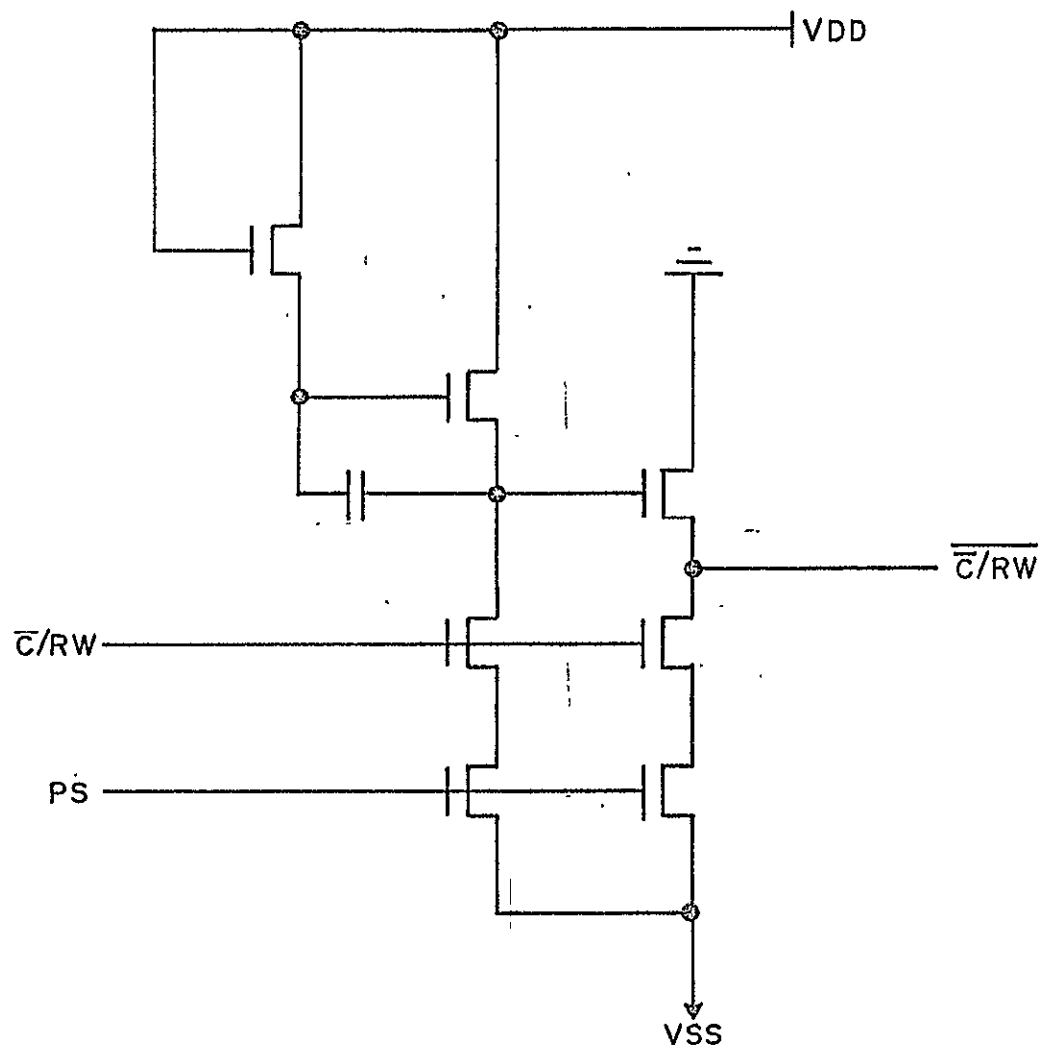
NASA RAM
CLEAR DRIVER CONTROL



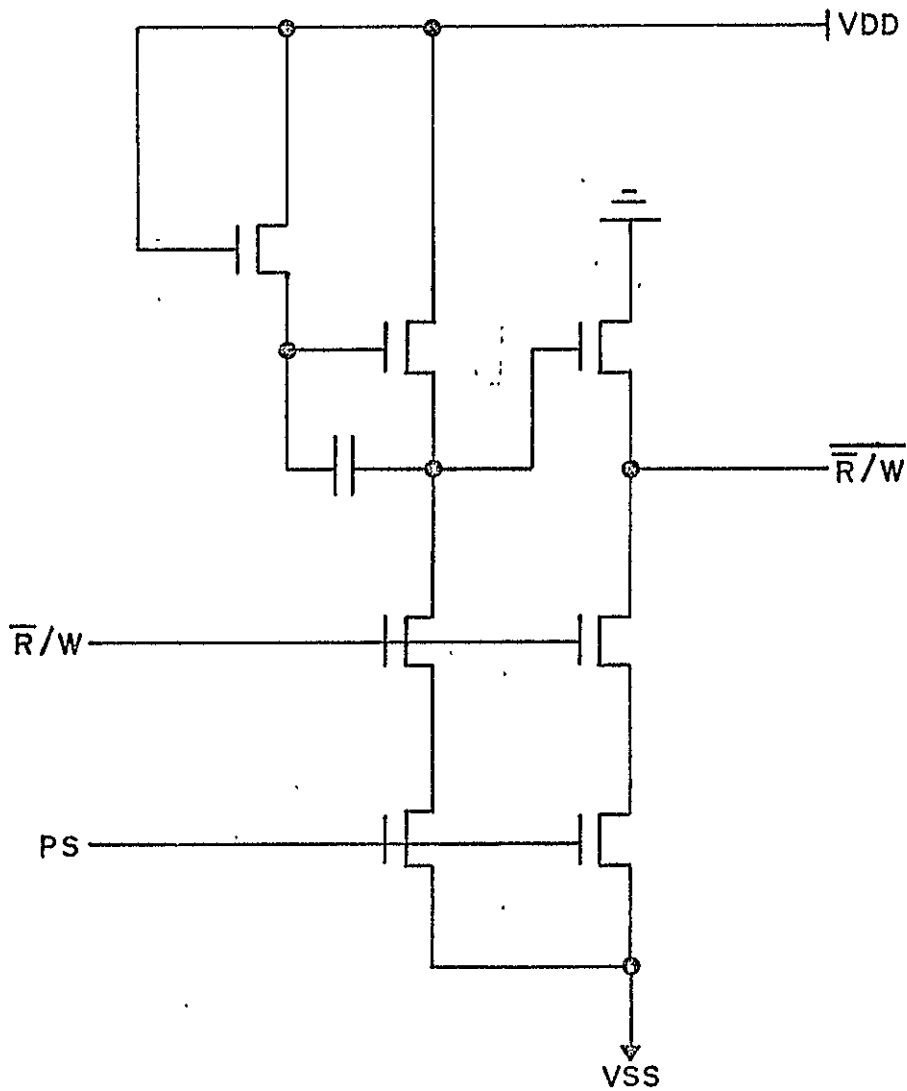
NASA RAM
TUB DRIVER CONTROL



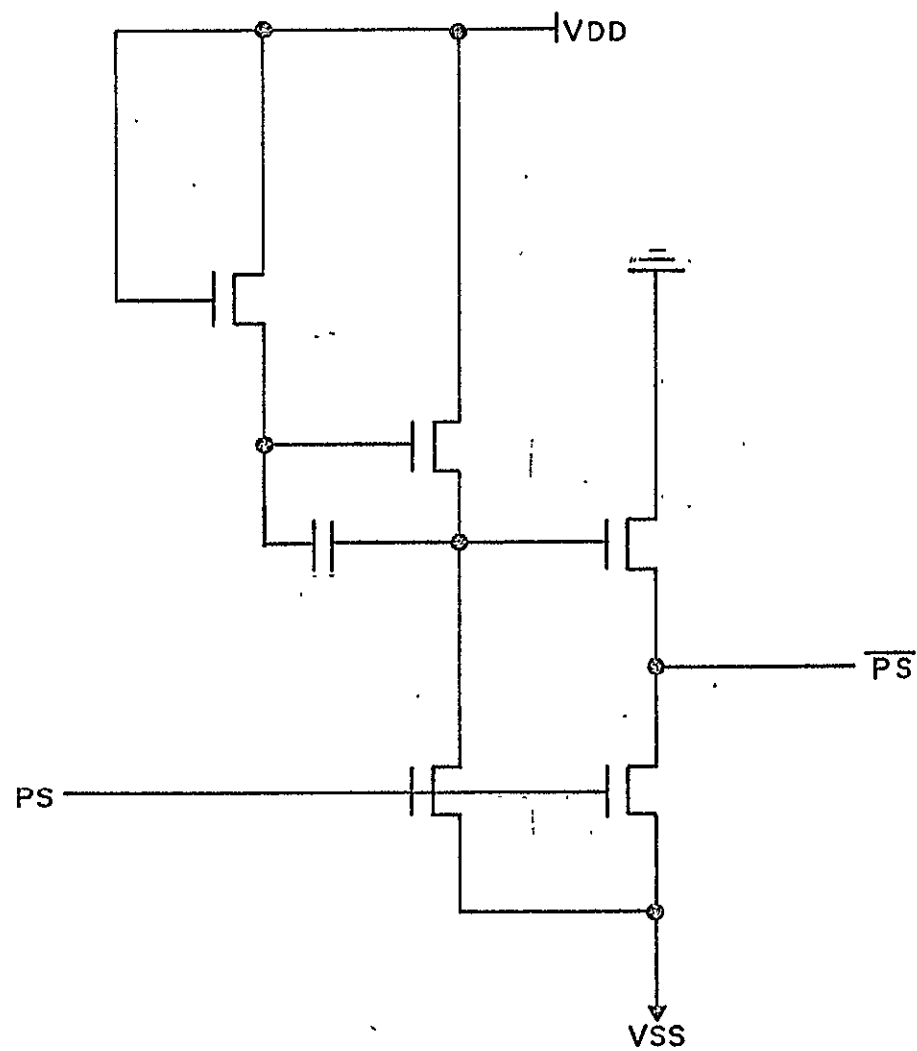
NASA RAM
CONTROL FOR READ POWER STROBE



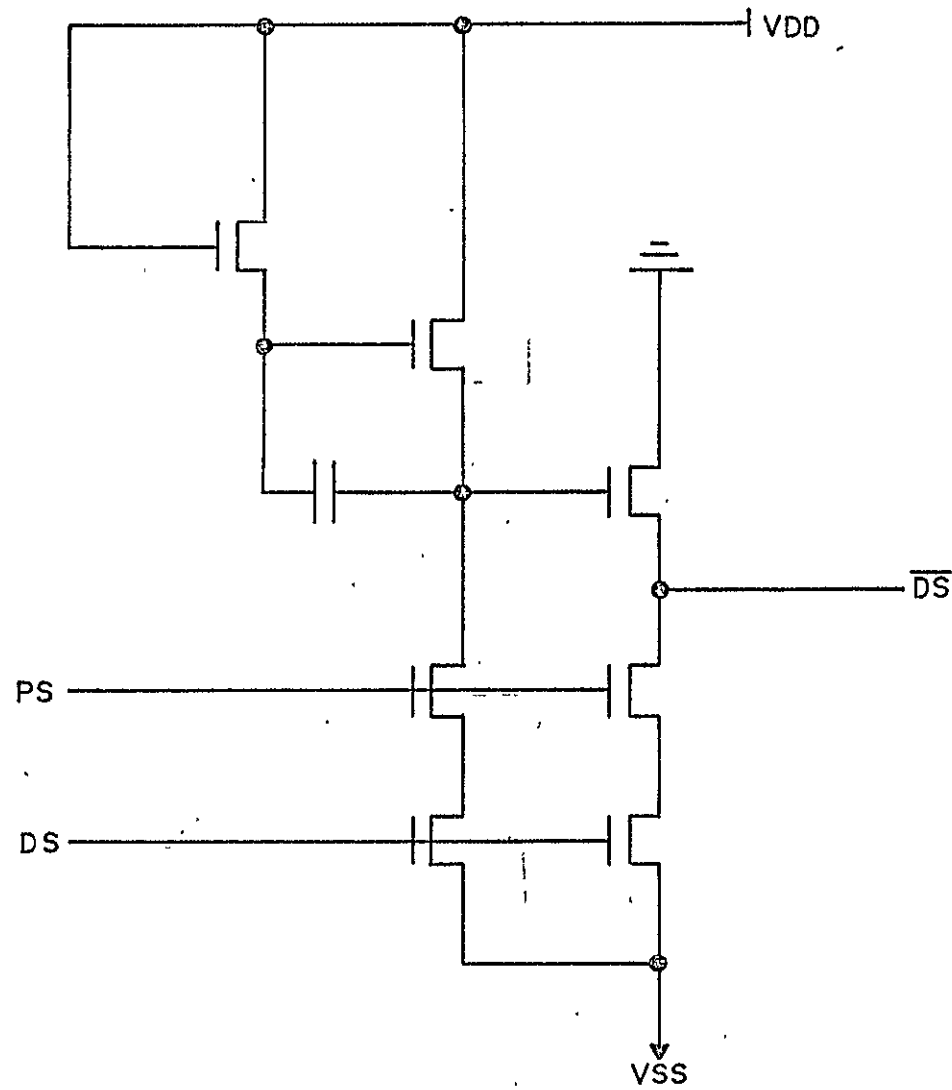
NASA RAM
CLEAR/READ WRITE BUFFER



NASA RAM
READ/WRITE BUFFER

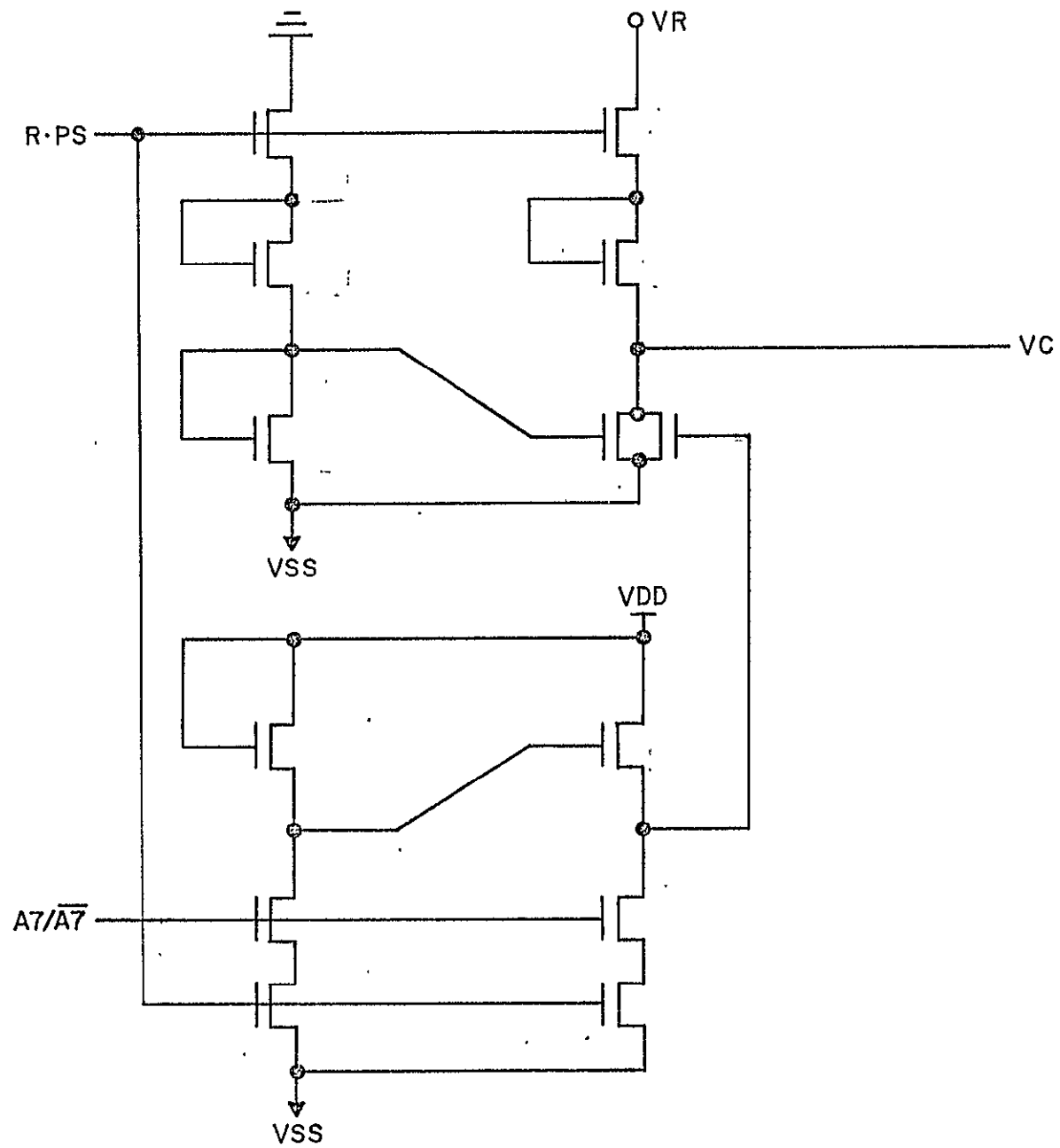


NASA RAM
POWER STROBE BUFFER

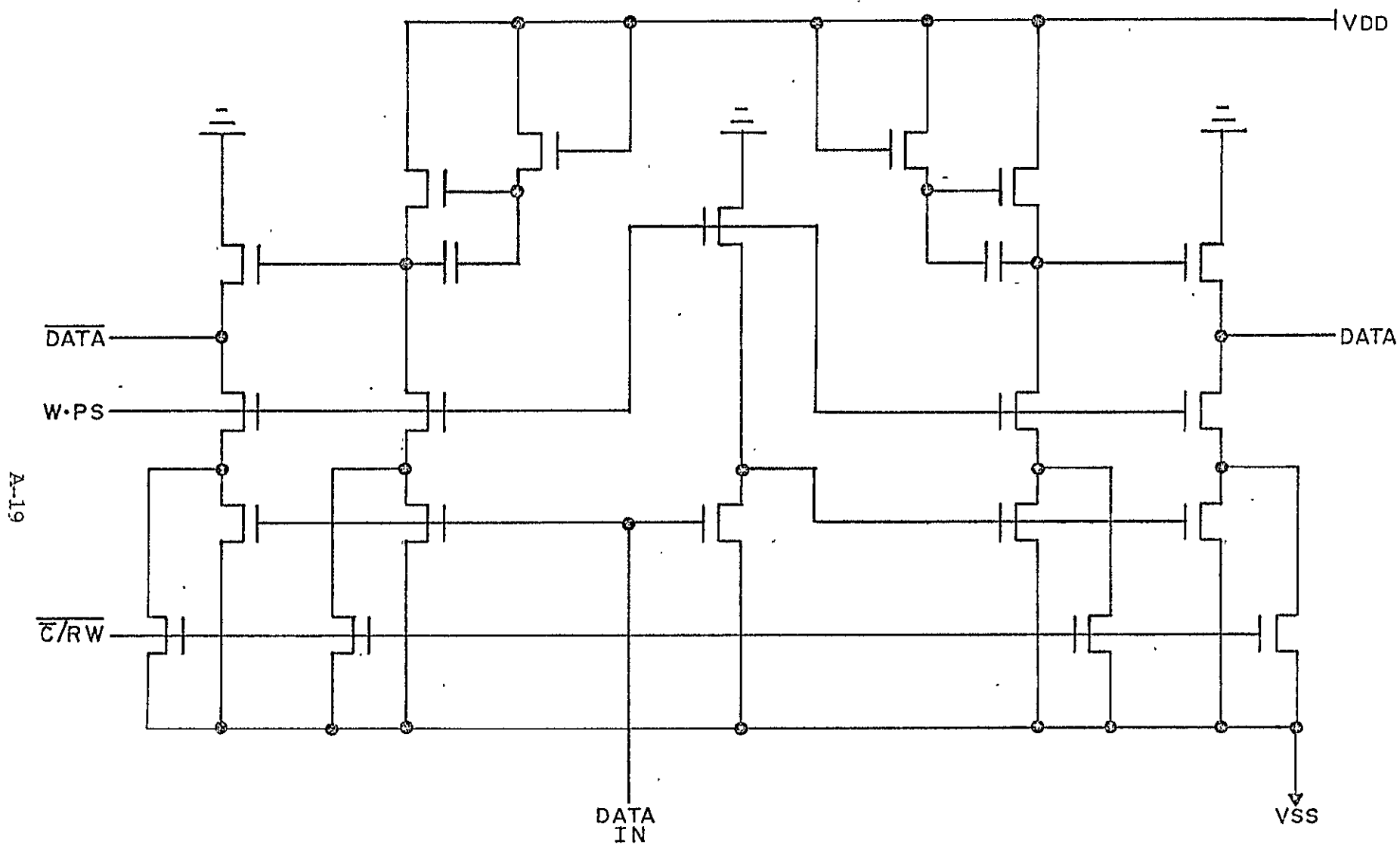


NASA RAM
DATA STROBE BUFFER

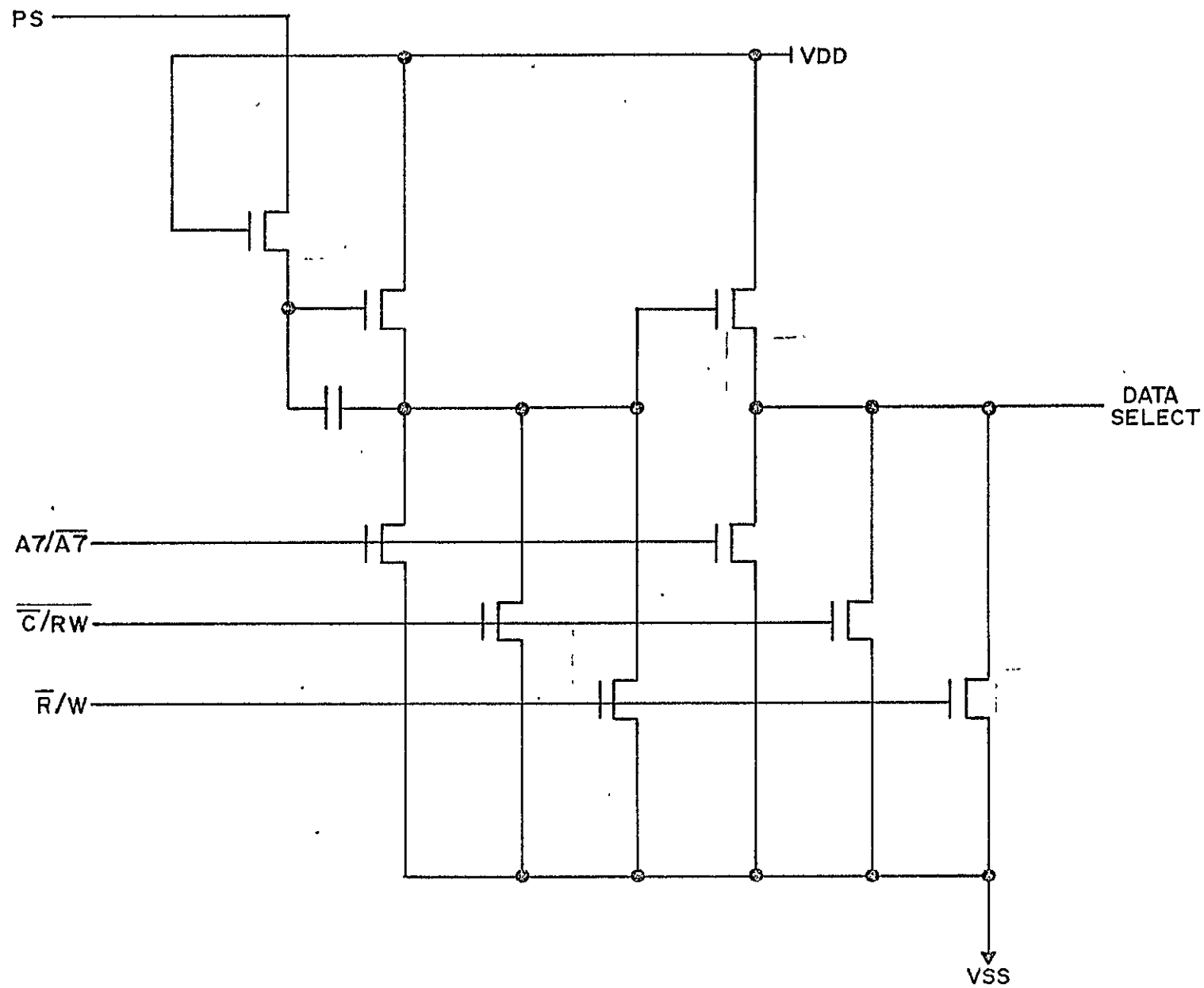
SENSE AMP AND OUTPUT BUFFER



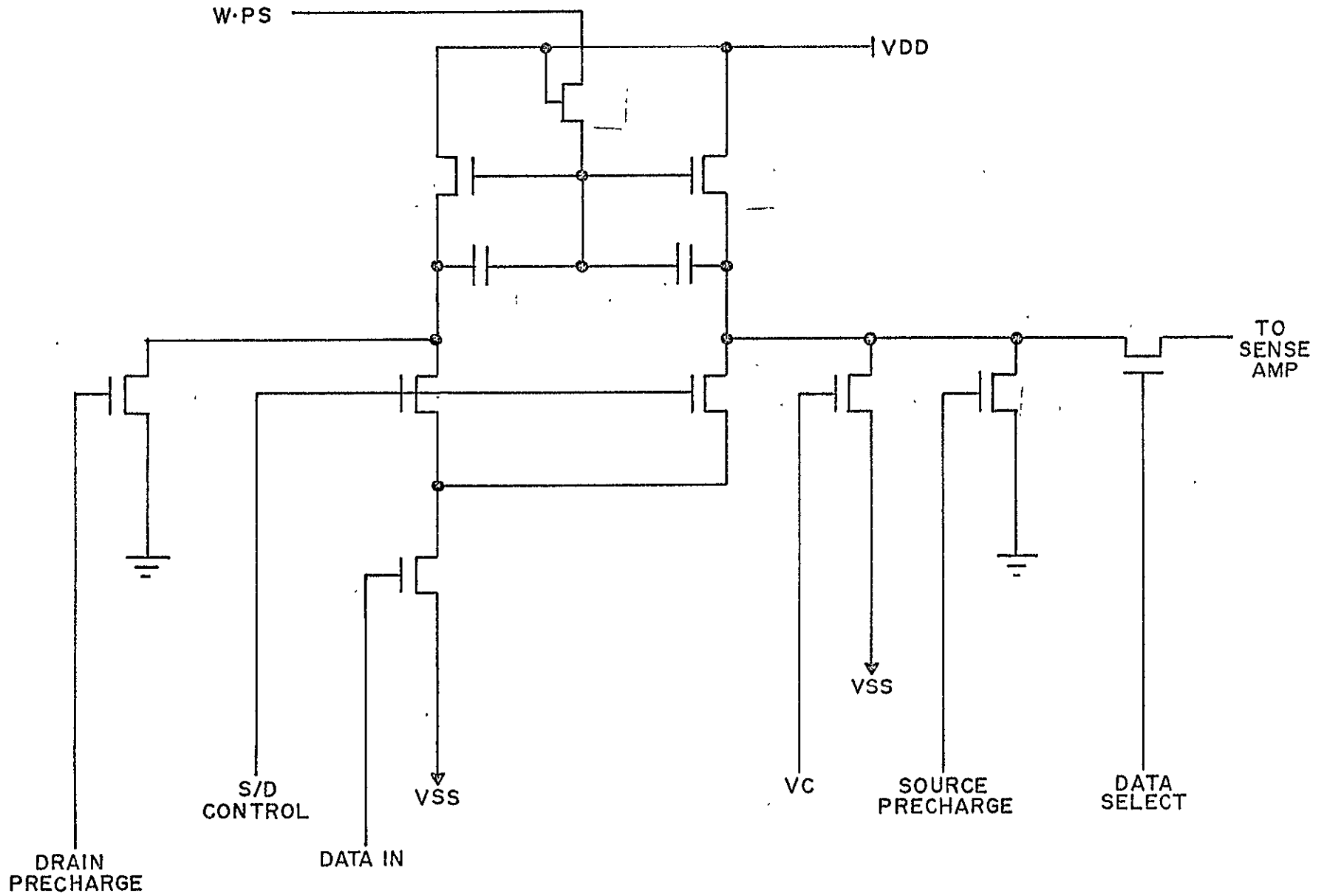
NASA RAM
VC GENERATOR



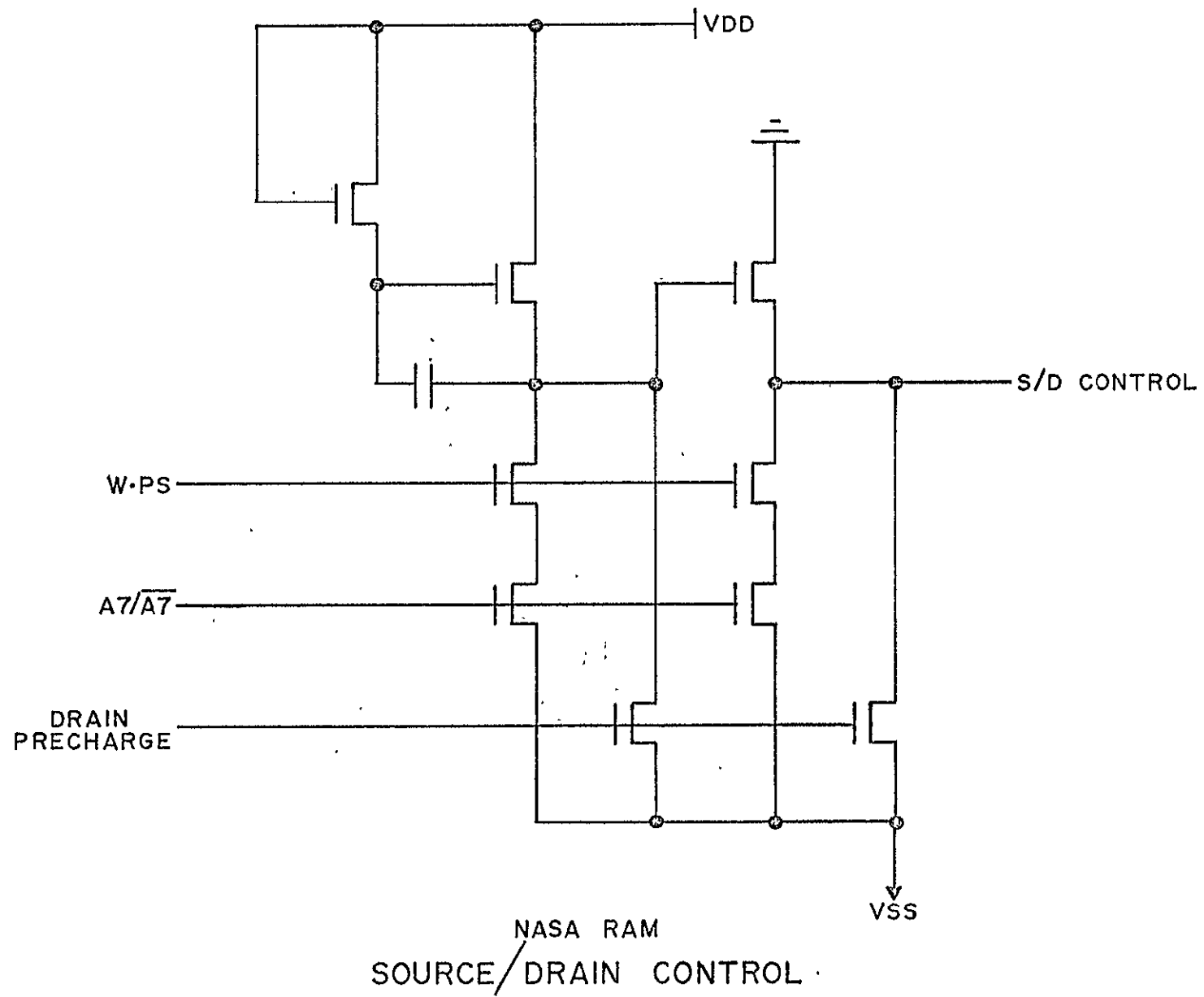
NASA RAM
DATA IN BUFFER

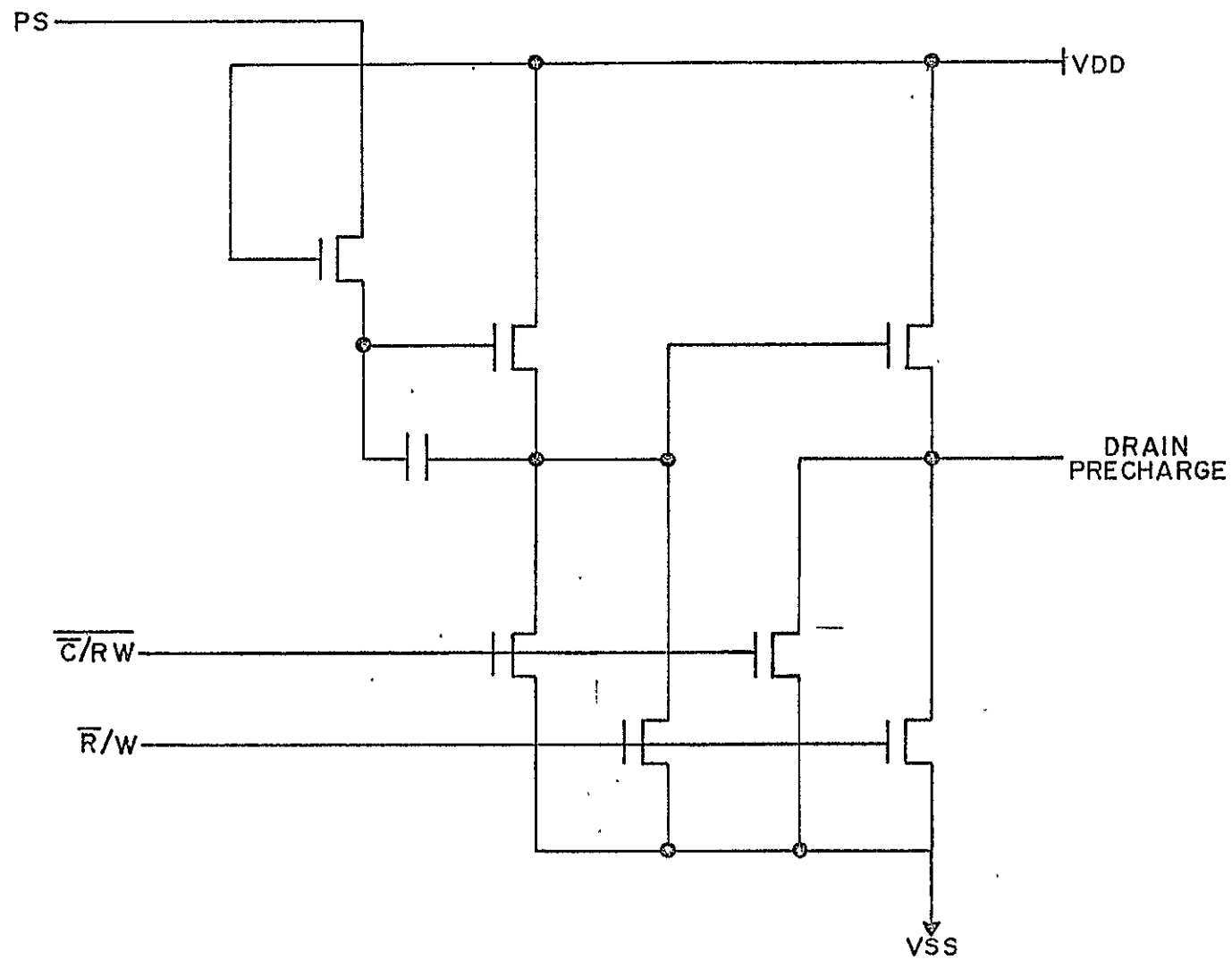


NASA RAM
DATA SELECT

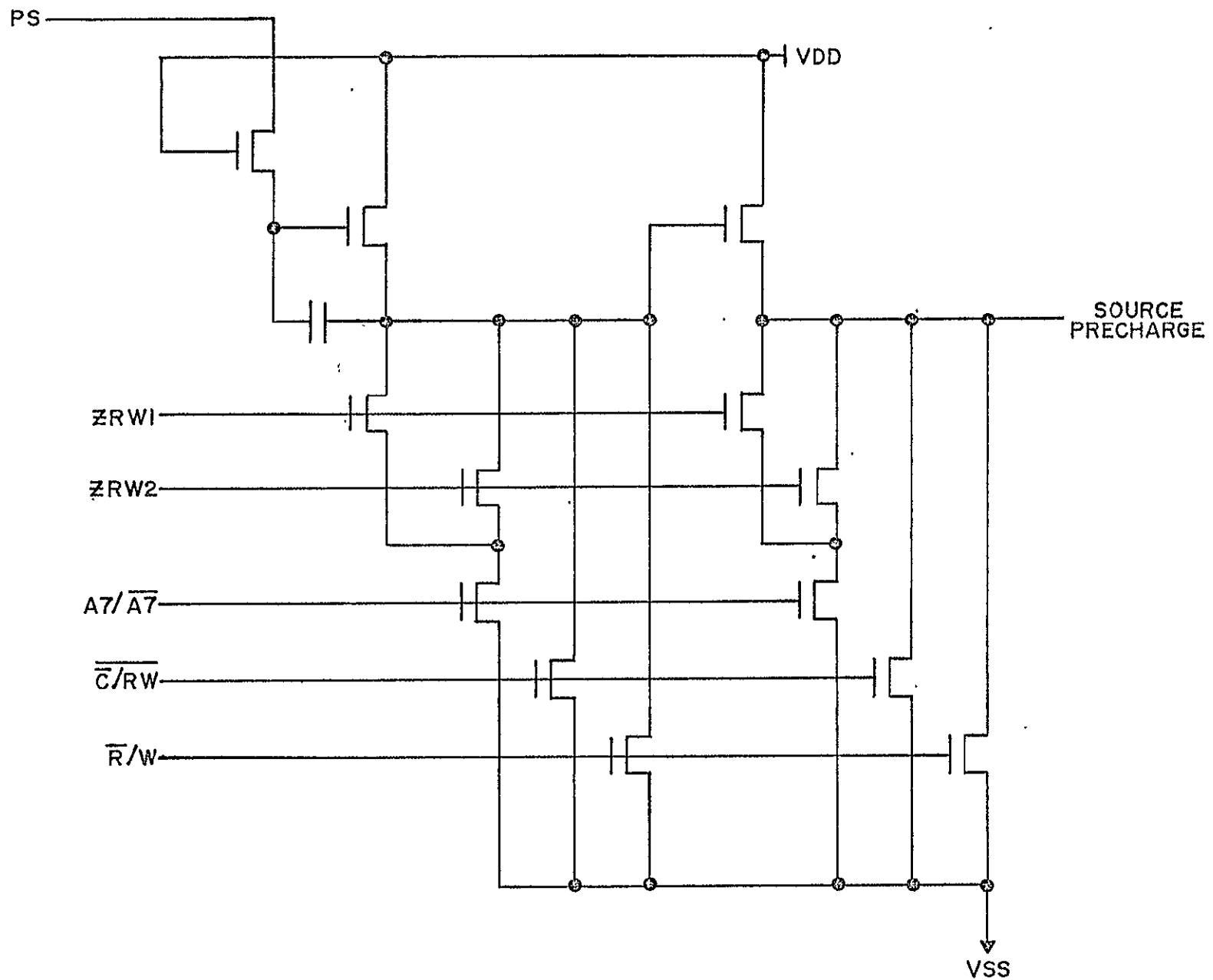


NASA RAM
SOURCE-DRAIN DRIVER



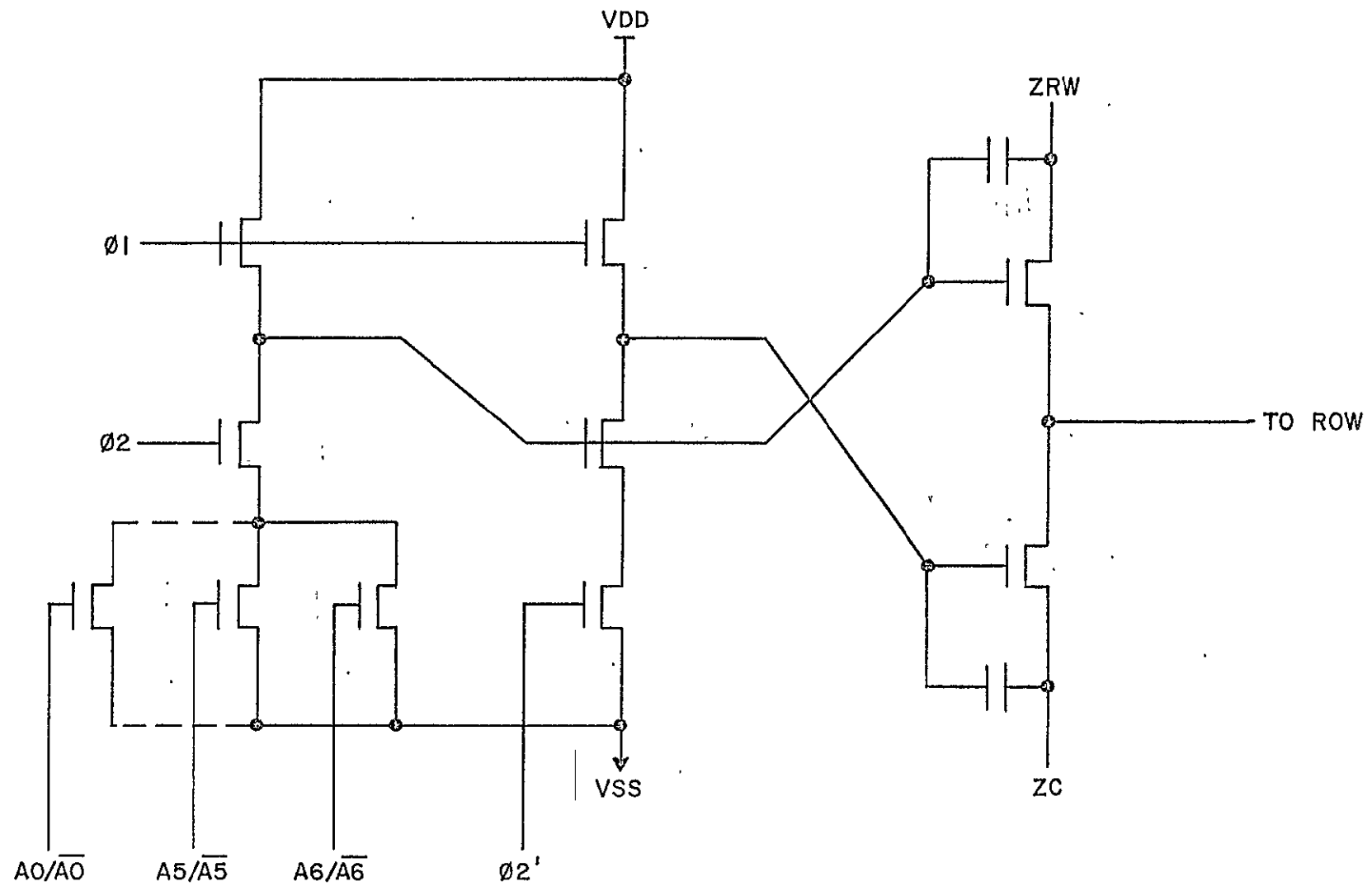


NASA RAM
DRAIN PRECHARGE

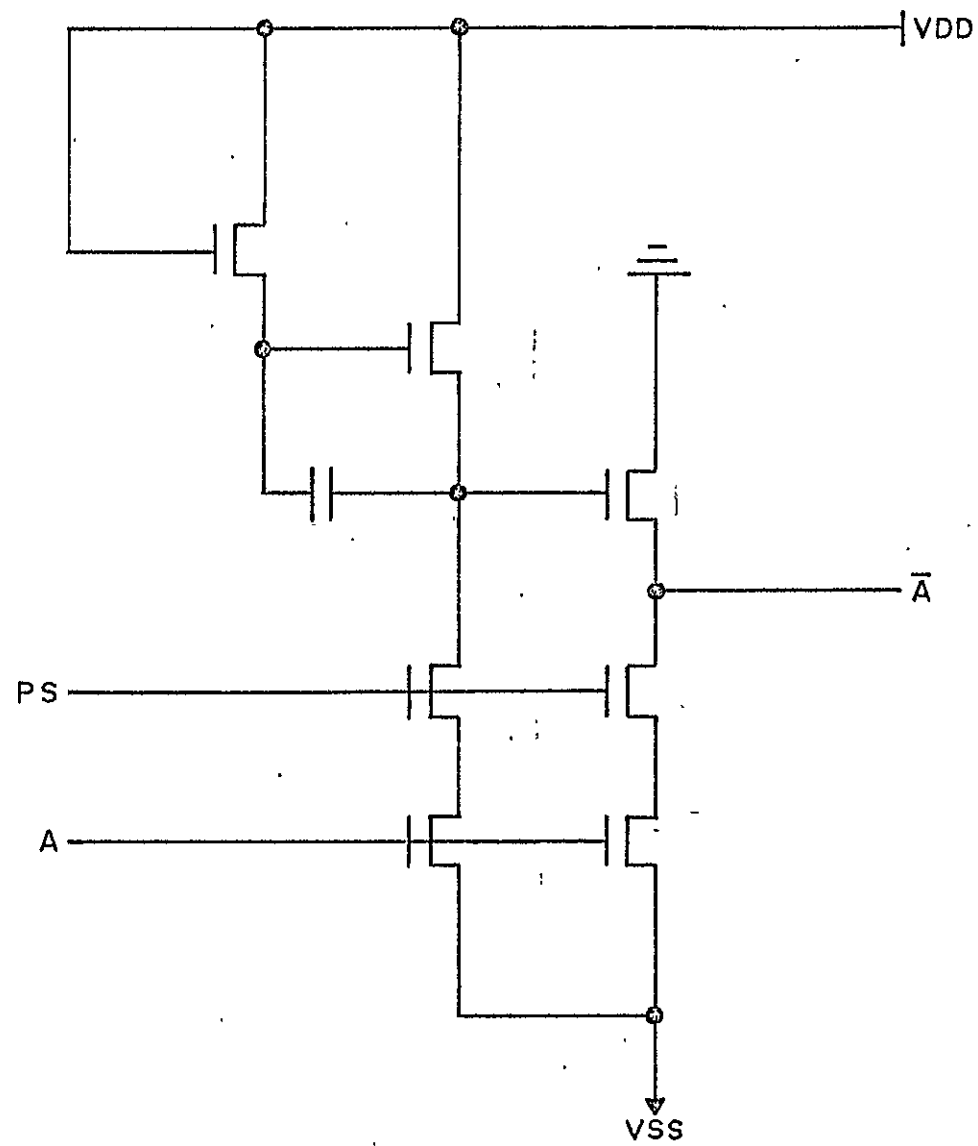


NASA RAM
SOURCE PRECHARGE

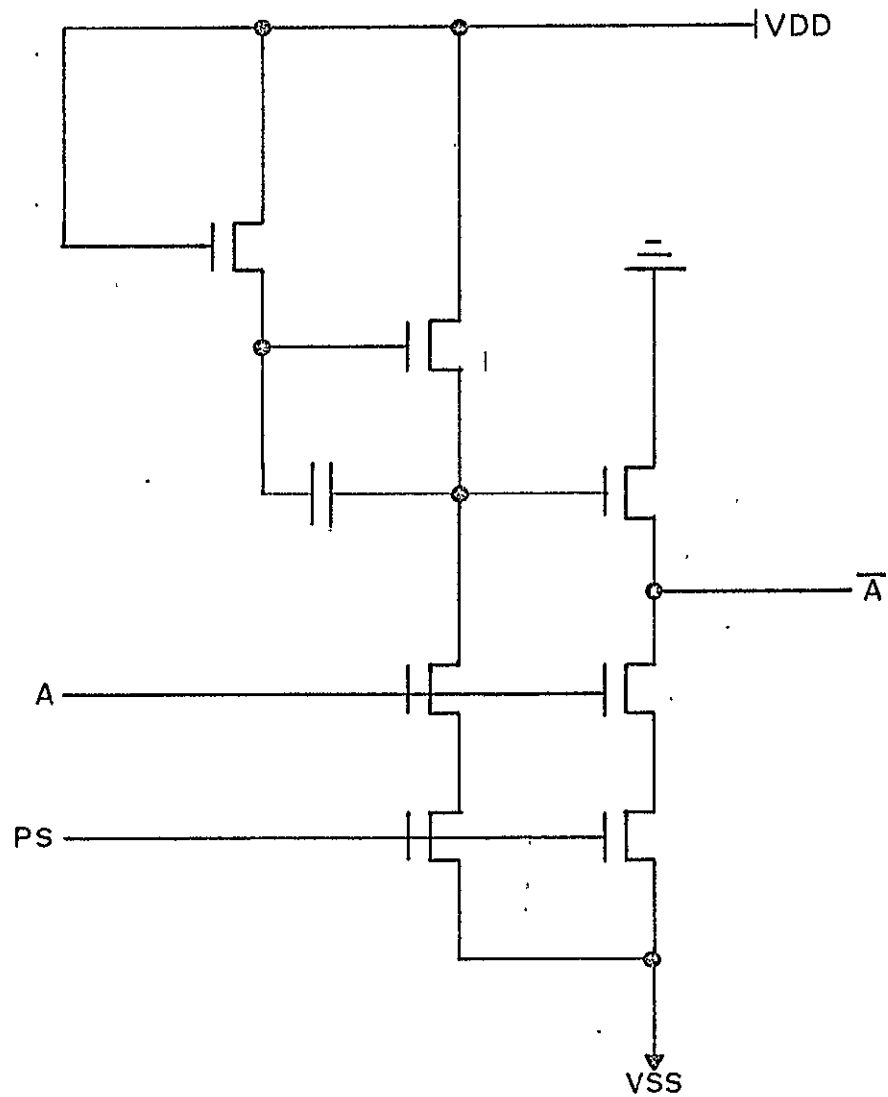
A-25



NASA RAM
ROW DRIVER



NASA RAM
ADDRESS INVERTER A7



NASA RAM
ADDRESS INVERTER (AO-A6)